

EE 414: Lab 4 – Frequency Synthesizer-based Local Oscillator

Abstract

This lab explores the design, construction, and testing of a frequency synthesizer based local oscillator (LO) to be used in the superheterodyne receiver block. Previous laboratory investigations looked at antennas, filters, and low noise amplifiers. Two voltage controlled oscillators and their respective PLL boards (referred to as Alpha and Beta) were constructed and tested. Locking was obtained at all five frequencies of interest (900MHz to 1GHz in 25MHz increments) though Alpha featured excellent high frequency performance, whereas Beta succeeded in maintaining sufficient output power at all frequencies while featuring insufficient spur suppression at only the 1GHz frequency. In both cases however, the frequency synthesizer LO was unable to perform at a single DC level shift voltage (used to match the output of the loop filter with the tuning range of the VCO). Phase noise measurements and spectrum analyzer results are shown.

Introduction

Local oscillators are an important component in wireless communication systems because they allow for the proper demodulation of a received signal. This lab explores the design, construction, and testing of a frequency synthesizer based local oscillator (LO) to be used in the superheterodyne receiver block. Previous laboratory investigations looked at antennas, filters, and low noise amplifiers. The following specifications were expected to be satisfied:

| Frequency Range | Output Power | Spur Suppression | Phase Margin |
|--|--------------------------------|------------------|-------------------|
| 900 MHz $\leq f \leq$ 1000 MHz In 25MHz intervals | > 0dBm 5 to 7 dBm preferred | ≤ -30 dBc | ≥ 45 degrees |

Table 1 - Specifications for VCO/PLL

Consisting of a phase locked loop and a voltage controlled oscillator, this LO can be programmed to generate a range of frequencies. Figure 2 shows the simplified block diagram for this topology used in this lab.

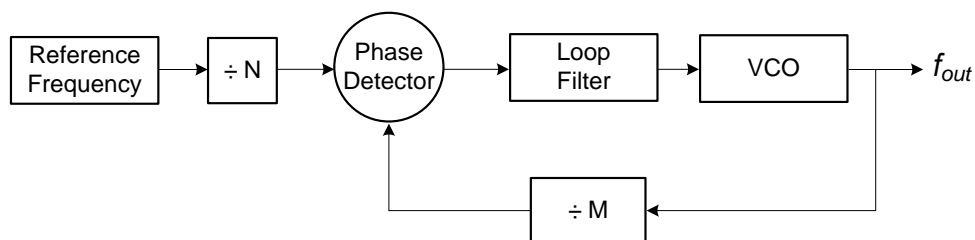


Figure 2 - Block model of the frequency synthesizer-based LO

This is a feedback control system in which the variable of interest is phase. This topology is known as a phase-locked loop (PLL) and is used to generate frequencies that are multiples of a given reference frequency. A quartz crystal resonator is used to provide a stable 25 MHz reference frequency. The phase detector block compares an incoming signal's phase to that of the reference and generates an output signal that is a function of the phase difference. This signal is conditioned by a loop filter before reaching the voltage controlled oscillator (VCO), which is an oscillator that produces an output at some frequency that is a function of the input voltage. The divider blocks, N and M , allow for the synthesis of different frequencies. They are related by:

$$\frac{f_{ref}}{N} = \frac{f_{out}}{M} \quad f_{out} = \frac{M}{N} f_{ref}$$

By adjusting the M divide factor, different output frequencies can be obtained. The various blocks in Figure 1 will be described in greater detail in the sections below. A note on terminology: though the architecture is known as a PLL, this lab features a partitioning between the VCO and ‘the rest of the PLL’. The former will still be referred to as the VCO, but the latter is often denoted as the ‘PLL board’. Also, two separate VCOs and PLL boards (Alpha and Beta) were constructed and tested and show different characteristics. Unfortunately, due to mechanical failure with Beta, there are incomplete results in terms of phase noise.

Frequency Synthesizer & PLL Board

This component of the lab involves the Motorola MC12181 integrated circuit which includes the phase detector, dividers, and charge pump for the PLL as well as the loop filter. Printed circuit boards were used to mount the IC, loop filter, DIP switch, crystal oscillator, and later the level shifter. A more detailed block diagram of the PLL is shown below in Figure 2.

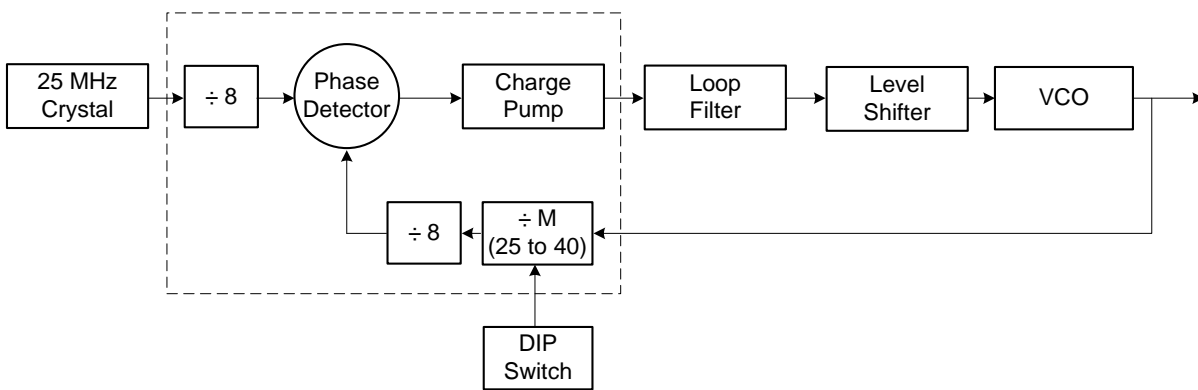


Figure3 - Detailed block diagram of PLL.

The dashed area indicates which components are contained inside the MC12181 chip. Prescalers of 8 are included in the reference frequency path and in the return path. A 25MHz quartz crystal oscillator loaded with two 15 pF capacitors and a 50k ohm feedback biasing resistor provides the reference frequency. The crystal was checked for third overtone operation by measuring it on a spectrum analyzer and this was confirmed not to be the case. The MC12181 supports 4-bit programming of the feedback path divider allows the user to select the desired frequency multiplier and ranges from 25 to 40. Using the

formula $f_{out} = \frac{M}{N} f_{ref} \rightarrow \frac{8 \cdot (25 \text{ to } 40)}{8} \cdot 25 \text{ MHz}$, this provides a range of 625MHz to 1000MHz. Integer

M values of 36 to 40 correspond to the five frequencies of interest, 900MHz to 1000MHz in 25MHz intervals.

A brief overview of the theory of operation: the phase detector compares the phase of the feedback signal to the reference signal. If the feedback signal is deemed ‘slow’, as in the VCO needs to increase its output frequency to provide the desired frequency as set by the DIP switch, a charge pump deposits charge onto a capacitor, thus increasing the control voltage to the VCO. If the feedback signal is too ‘fast’, an ideally equal and opposite charge pump removes charge, lowering the control voltage to the VCO. The loop filter contains this capacitor performs further signal conditioning. A resistor provides a loop-stabilizing zero and is included in series with the integrating capacitor. Injected noise into the control voltage line and asymmetries in the charge pump or phase detector can be periodic in nature and thus produce sideband spurs. The loop filter should also smooth out the characteristic ‘sawtooth’ pattern response of the phase

detector. Higher order filters are naturally more complex and greater care is needed to ensure stability. It has been found that while a fourth-order loop filter is optimum, a third-order filter is sufficient and is more straightforward to design. A loop filter design tool by National Semiconductor (*PLL_LpFtr*) was used to design a third-order filter, shown in Figure 4.

The tool requests a charge pump current I_C , VCO gain constant K_{VCO} , loop bandwidth, divider, phase margin, and desired spur attenuation. $I_C = 2.2\text{mA}$ from the datasheet, and since the VCO was currently in development, a gain constant of 20 to 25 MHz/V (22 MHz/V actual) was estimated for K_{VCO} . Though a 45 degree phase margin was specified, we expected degradation in the phase margin in the process of realizing the circuit, so the loop filter was over-designed to 56 degree phase margin, and for the same reason the attenuation was set at 40 dB. The loop bandwidth was another parameter was iterated. The loop bandwidth plays a critical role in the transmitter block, and has to do with how fast the loop acts. A bandwidth of 100 kHz was initially chosen but then increased to 200 kHz after it was suspected that the loop filter was not reacting fast enough to acquire and maintain a lock.

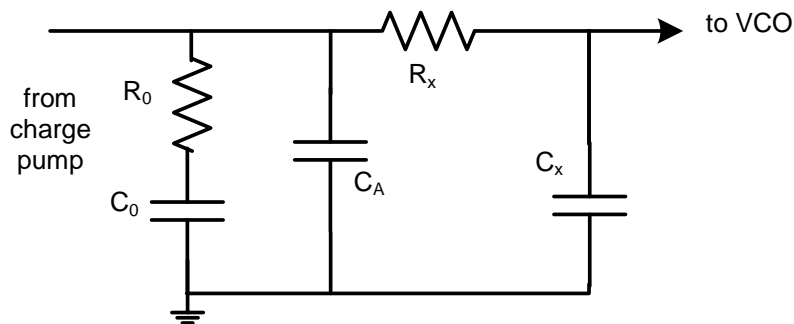
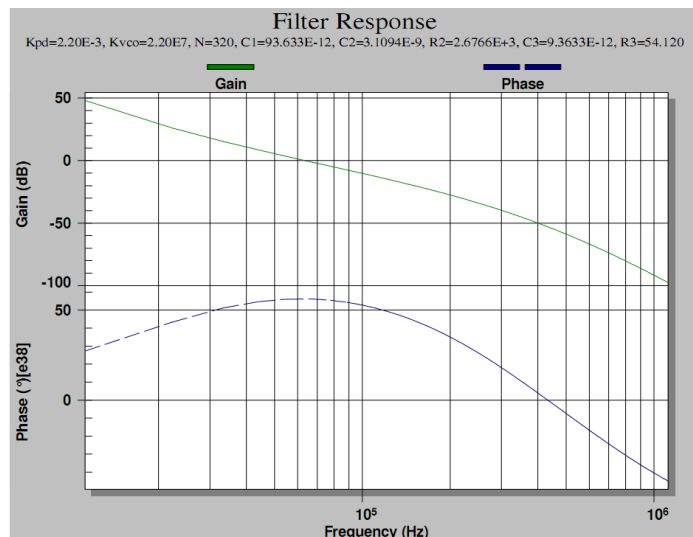


Figure 4 - 3rd Order Loop Filter

The values obtained by the loop filter and the actual values used are shown along with the frequency response of the filter in the table and figure below.

| Component | Designed Value | Actual Value Used |
|-----------|----------------|-------------------|
| R_o | 93.6pF | 94pF |
| C_o | 3.1nF | 3.0nF |
| C_A | 2.68k | 2.67k |
| R_X | 54.1k | 54.9k |
| C_X | 9.36pF | 9.4pF |

Figure 5 - Component values for Loop Filter and Frequency Response



Another important issue that had to be addressed was the loading of the VCO due to the PLL board. The output signal of the VCO is tapped to create the feedback system. This tapped signal is tied to the F_{in} pin on the MC12181 and is fed into the prescaler, frequency multiplier, and finally to the phase detector. This pin has a parasitic capacitance of a couple picofarads and is ac-coupled to the feedback signal through a large DC blocking capacitor. A VNA was used to characterize the F_{in} pin and a Smith chart is shown in Figure 6.

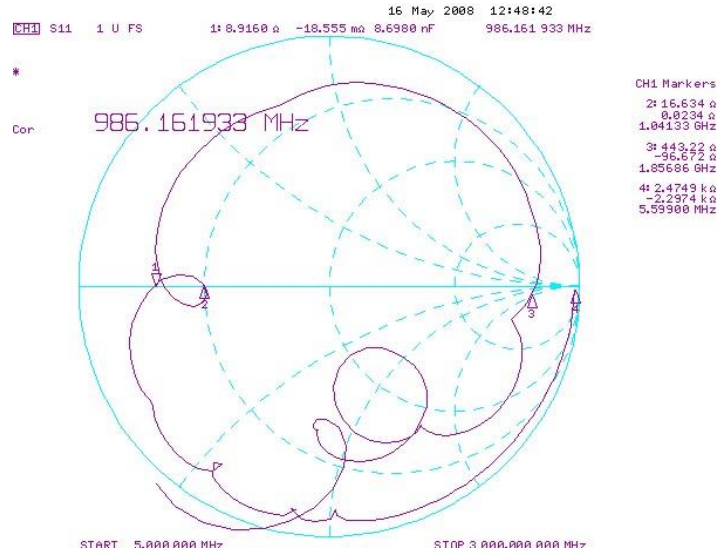


Figure 6 - S_{11} of the Fin pin on MC12181 Frequency Synthesizer

Of particular interest is the region on the horizontal terminator on the left (open) side of the Smith chart. There is a zero-reactance line crossing at 986MHz and 1041MHz. One idea suggested by Siddharth Seth was to create a through path using two BNC connectors connected with a 50 ohm transmission line and then capacitively tapping that line to the F_{in} pin. The f_{out} of VCO would connect to one BNC and the line to the spectrum analyzer would be connected to the other. This method was attempted on both boards, with slight changes in the layout. Both constructed boards are shown below in Figure 7 and Figure 8.

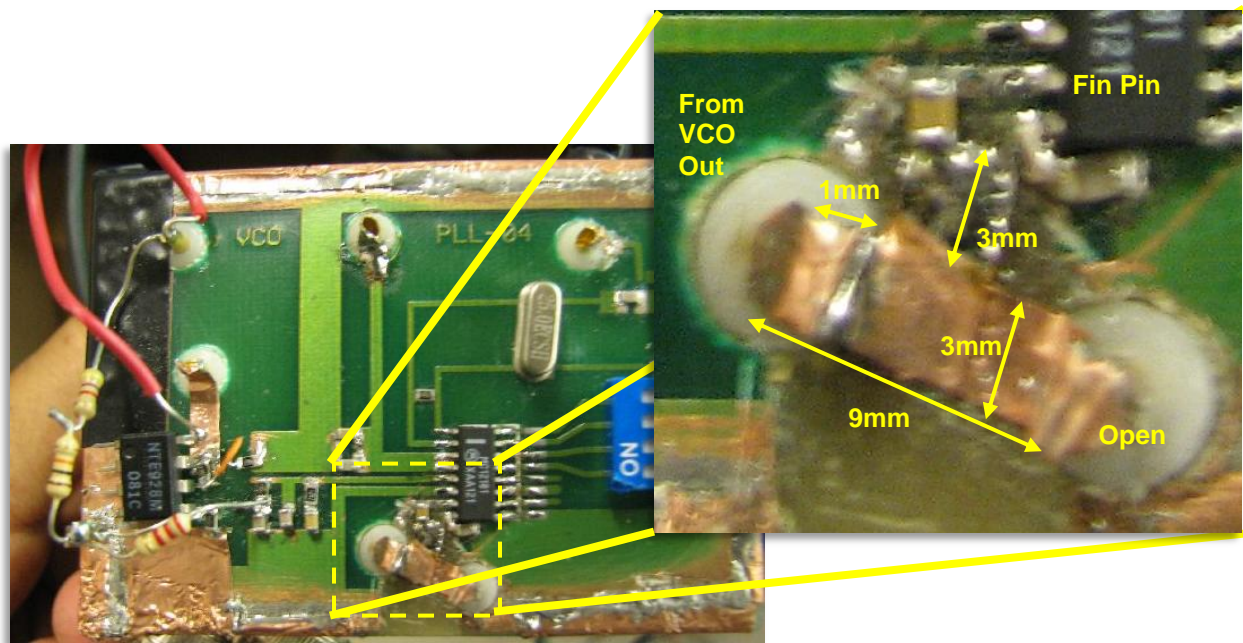


Figure 7 – Alpha's PLL Board

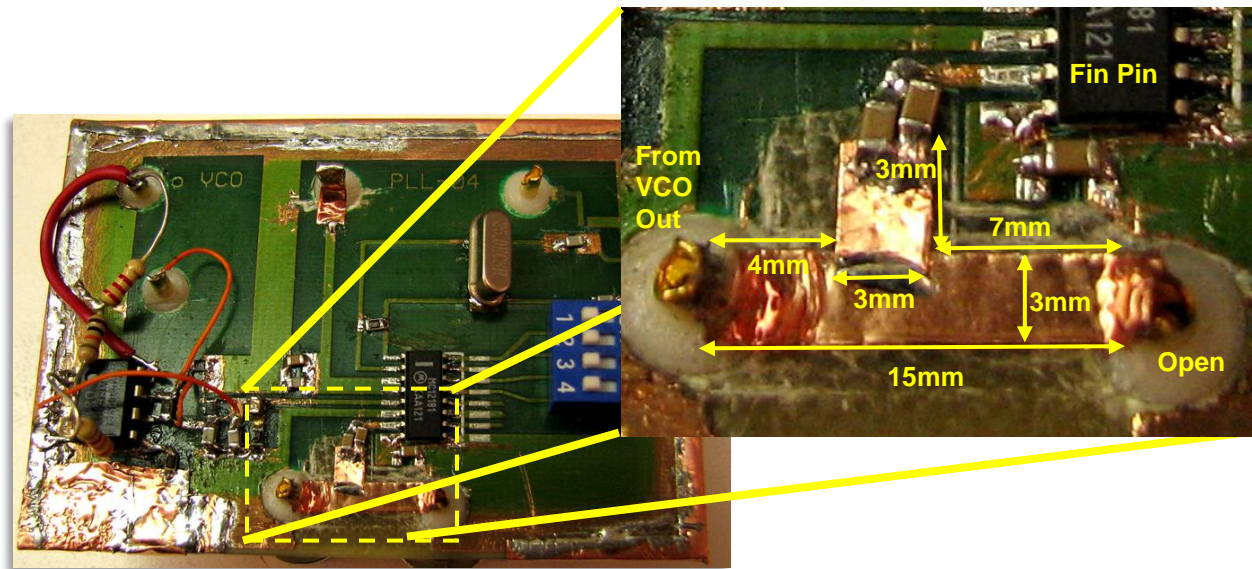


Figure 8 – Beta's PLL Board

Alpha's board was the first one to try the transmission like idea and poor construction technique made it difficult to create a clean tap. Beta's board was newer and thus shows a better tap. Alpha's board uses 1nF capacitor as the DC block, Beta's board uses two 1nF for greater physical geometry matching.

Through testing, it was deemed that the method was actually degrading performance and if the other BNC connector was left open, the PLL locked and maintained sufficient output power. Presumably, the F_{in} does not need large amounts of signal power to function, and so maximum power transfer is not required.

Voltage Controlled Oscillator

A Colpitts oscillator topology, a positive feedback system that is capacitively tapped, was chosen for the VCO and is shown in Figure 9.

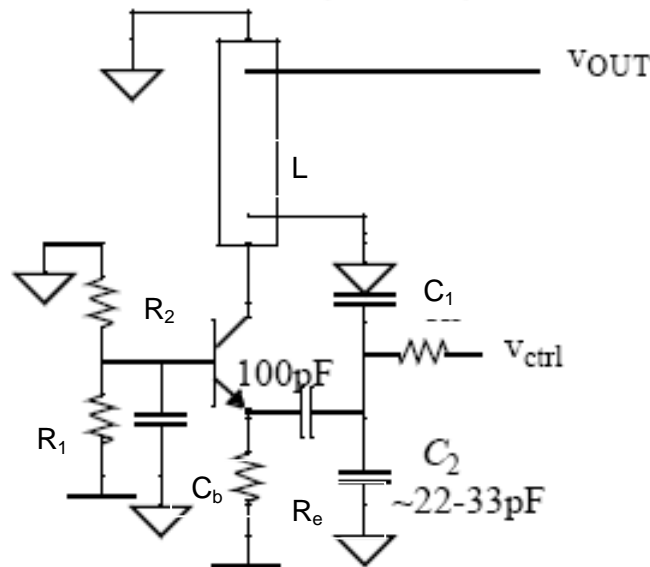


Figure 9 - Initial Topology for Colpitts Voltage Controlled Oscillator

Voltage control is provided by using a varactor that adjusts an LC tank's capacitance and thus frequency of oscillation. This control voltage is supplied by the Motorola MC12181 chip (described below) and is constrained to a 0.5V to 4.5V range. We began based on the assumption that this would directly act as the control voltage for the varactor diode, which can be tuned between 8pF to 18pF in that voltage range.

The effective capacitance of the tank is given by the series combination of C_1 and C_2 and is thus given by $\frac{C_1 C_2}{C_1 + C_2}$. For very large values of C_2 the capacitance then approaches C_1 and this is what we want. In

order to be able to control the tank capacitance we need C_1 to dominate the total tank capacitance and hence C_2 was chosen to be 22 pF because under all circumstances it will be greater than C_1 and since we are targeting relatively large frequencies it is prudent to not make any the capacitance in the tank unnecessarily large. Making C_2 extremely large would prove detrimental because this capacitor acts as a feedback capacitor and the principle on which the oscillator works is that this capacitor is charged when the transistor is on and the moment the capacitor voltage rises high enough then the base-emitter junction is no longer forward biased, and the transistor switches off. As the charge from the capacitor diminishes and the base voltage rises above the emitter voltage the junction is forward-biased again and the transistor begins operation. If the capacitor is so large that it does not lose charge quickly then in the next cycle when the voltage at the base again rises it would not be sufficient to forward bias the base-emitter junction.

The most challenging aspect of building the oscillator was to obtain the right inductance for the tank circuit. We now compute an estimate of the inductance that we need to have oscillation from 900MHz to 1GHz. Assuming there is about 4 pF of parasitic capacitance at the emitter of the transistor being contributed by C_π that gets added in parallel of C_2 , the total capacitance of the tank varies from $(8||((22+4)))$ pF = 6.11pF to $(18||((22+4)))$ pF= 10.63pF when the control voltage goes from 0.5 V to 4.5 V. The average of these values is around 8pF and that is where we want our center frequency to be tuned. In this lab we are trying to achieve a tuning range from 900 MHz to 1 GHz so the center frequency is 950 MHz. The

corresponding inductor value is given by $L = \frac{1}{\omega^2 C_{tot}}$, where C_{tot} is 8pF and ω is 5.96 Grad/s. The

inductance therefore needs to be around 3.5nH. If we make the naïve assumption that we are not picking up any parasitic inductance from the components leads and solder etc. then we can compute the length of the transmission line that we need to provide this much inductance from the following equation that is derived from the impedance transformation equation for a load much smaller than the characteristic impedance of the transmission line, i.e., $Z_L \ll Z_0$. This conditioned is obtained by shorting one of the ends of the transmission line to ground.

$$Z(z) = Z_0 j \tan(\beta l) \text{ or } L = \frac{Z_0 j \tan(\beta l)}{2\pi f_0}, \text{ where } Z_0 \text{ is } 50 \text{ ohm, } f_0 \text{ is the center frequency, and } \lambda \text{ is the}$$

wavelength of a 950 MHz wave on the FR4 board and is equal to $300 \text{ mm} \times 0.5434 = 163 \text{ mm}$. The length of the line, l , that we get from the above computation is approximately 9 mm. While performing the above calculations we realize that the impedances required are small enough that $\tan(\beta l) = \beta l$, implying a linear relationship between impedance and length of the line, so it is reasonable to state that we get 1 nH from every 3 mm of 50 ohm copper strip on FR4.

It must be mentioned that choosing a wider line which has characteristic impedance less than 50 ohm allows us to use a longer strip of line but that results in a drop in the Q factor of the inductance that we are trying to obtain and it does not result in an inductor as good as we desire.

The output of the oscillator, V_{tank} , is given by

$$V_{\text{tank}} = 2 I_{\text{BIAS}} R_{\text{tank}} (1-n),$$

where R_{tank} is the tank load and $(1-n)$ is the multiplicative factor that has to be included because that comes from the large-signal input resistance of the transistor that is reflected from the capacitive impedance transformer and adds to the load of the tank. Here n is given by $C_1/(C_1+C_2)$.

The requirement for oscillations to occur is that the loop transmission magnitude should be greater than unity and another way of expressing that is that $g_m > 1/R_{\text{tank}}$ [$n \cdot n^2$]. Combined with the equation of V_{tank} mentioned above, this equation can help us choose the right bias current, I_{BIAS} , that would ensure that oscillations occur for the chosen I_{BIAS} and we meet the specified output power between 0-7dBm or 1-5

mW. This implies $1mW < \frac{V_{\text{out}}^2}{2 \cdot 50\Omega} < 5mW$ or $0.316V < V_{\text{out}} < 0.707V$. The challenge then is to tap the

transmission line such that resistance looking into the tap point is 50 ohm so that maximum power can be transferred and then compute the corresponding load seen by the tank, R_{tank} , through the inductive impedance transformer. This can be computed using the equation for tapped impedance transformer formed by the inductive transmission line we have at the collector of the transistor under the assumption that Q of this transformer is much greater than 1. We get the following equation for resistance looking into the output port, R_{tap} , of the oscillator

$$R_{\text{tap}} = \left(\frac{L_1}{L_1 + L_2} \right)^2 R_{\text{out}} \quad \text{where } R_{\text{out}} \text{ is the output resistance of the transistor seen by the impedance}$$

transformer at the collector node of the transistor and L_1 and L_2 are the inductance values above and below the tap point. In this case R_{out} is given by $r_o(1+g_m R_e)$ and for $g_m R_e \gg 1$ it reduces to $r_o g_m R_e$, where $r_o = V_A/I_c$ and $g_m = I_c/V_T$. V_A is the early voltage and V_T is the thermal voltage. Therefore

$$R_{\text{out}} = \frac{V_A}{I_c} \frac{I_c}{V_T} R_e = \frac{V_A}{V_T} R_e = \frac{50}{.025} R_e = 2000 R_e$$

If we can choose an appropriate tap point and hence L_1 and L_2 , we can transform the R_{out} above to $R_{\text{tap}} = 50$ ohm to get maximum power transfer. And due to reciprocity of the network the 50 ohm load, R_{tap} , will be transformed to R_{out} at the collector node (the node with V_{tank} potential) and R_{tank} becomes $R_{\text{out}} || R_{\text{out}} = R_{\text{out}}/2$ (it own output resistance and the one transformed from the load combined in parallel with each other). However this entire procedure hinges on the aforementioned assumption of $Q \gg 1$ or $\omega L/R_{\text{tap}} \gg 1$ or $\omega L \gg 50\text{ohm}$ or $L \gg 8\text{-}9 \text{ nH}$. This is certainly not the case and thus we cannot follow this procedure to compute the right tap point, hence R_{tank} followed by I_{BIAS} and V_{tank} to meet our power requirement and oscillation requirement. Thus we simply follow the procedure suggested in the text. We first choose a bias voltage of -8 V to so that we have some margin later to increase it if there is a need to increase the bias current. We then assume a current we wish to bias our oscillator at and that we choose based on the efficiency that we expect from our oscillator. Given that we need a maximum of 7 dBm output power which translates to 5 mW and we expect about 10% efficiency then our static power dissipation should be around 50 mW. So for a 8V supply the bias current is 6.25 mA. Now to bias the circuit at this current we assume that we drop 2V across the emitter resistance, R_e , which comes out to be $3/6.25\text{mA} = 320 \text{ ohm}$. We then assume about $1/10^{\text{th}}$ of the bias current flows through the biasing transistors R_1 and R_2 (with the assumption that base current is zero) The voltage drop across the two resistors is 8 V and therefore the sum of two resistors, (R_1+R_2) , is $8V/6.25 \text{ mA} = 12800 \text{ ohm}$. Since we dropped two volts across the emitter resistance the emitter voltage is given by -6 V and if 0.75 V drop occurs from the base to emitter then the base voltage is -5.25 V. So using the voltage divider equation we can compute $R_1/(R_1+R_2)=5.25/8$. We then get $R_1=8400 \text{ ohm}$ and $R_2=4400 \text{ ohm}$.

We use 1 μF bypass capacitor at the base of the transistor and, as suggested in the text, use 1 k Ω resistance between the control voltage and the cathode of the varactor.

Few attempts with the copper strip acting as the inductor reveal that the parasitic inductance is too high and the parasitics are enough to provide the $\sim 3 \text{ nH}$ we are looking for. So taking the advice of the TA we simply used the collector lead of the transistor to act as our inductance. Despite doing that we found it difficult to reach 1 GHz range. So to push the frequency up we reduced the value of C_2 to 5 pF from previously chosen 22 pF. When even this did not work we completely removed this capacitor and used

the inherent capacitance of the transistor as our C_2 . We see that C_{π} is almost 10 pF from the equation for diffusion capacitance $C_b = \frac{I_c}{V_T \omega_{T,peak}}$ and that is ample for our requirements. We must also mention that

extreme care was taken in the physical layout of the oscillator, as seen in Figure 10. No wire or transmission line was used to connect two components in the circuit and they were all placed right next to each other and connected by means of solder. R_e was later changed from 320 ohm to 150 ohm to roughly double the current to improve output power. The final constructed VCO by Panwar is shown in Figure 10.

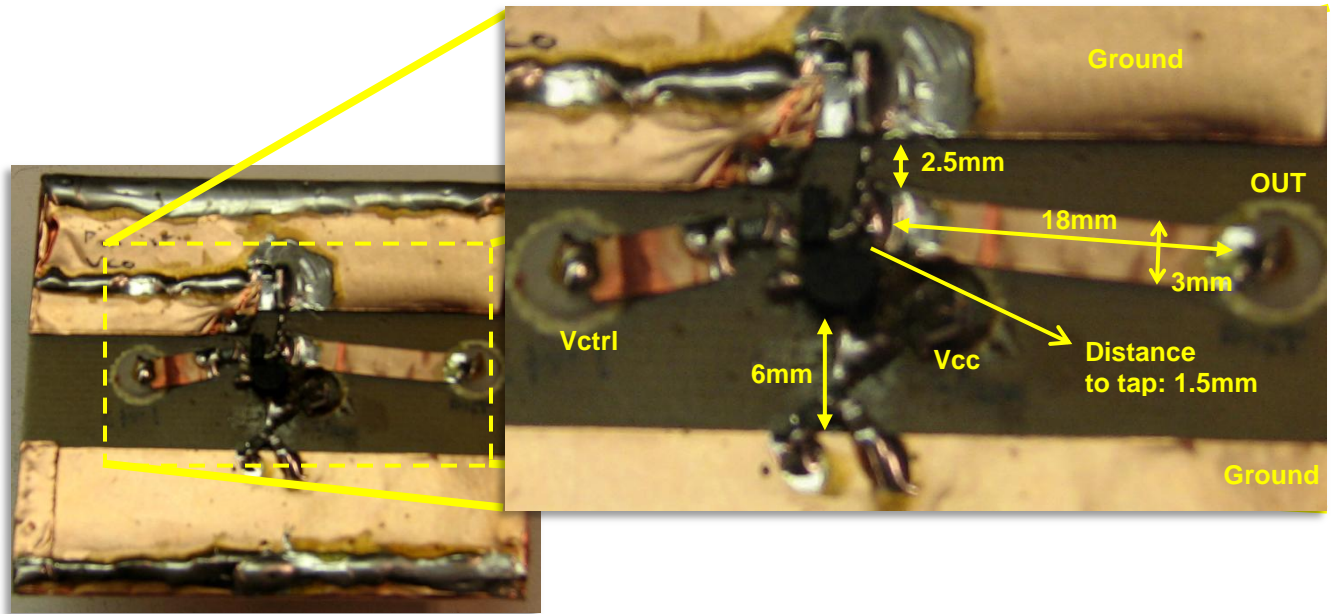


Figure 10 - Beta's VCO

The above design prescription reflects the choices made for Beta's VCO. Chen built a separate VCO utilizing the same key principles – removal of C_2 capacitor due to presence of parasitics and using the collector lead to provide the tank inductance. Next, the VCOs were characterized for their output power and frequency range versus control voltage sweep, known as tuning curves.

A VCO meter was used to provide a sweeping control voltage and to measure the output of the VCO. The tuning curve for Beta's VCO is shown in Figure 11. This was measured with the standalone VCO.

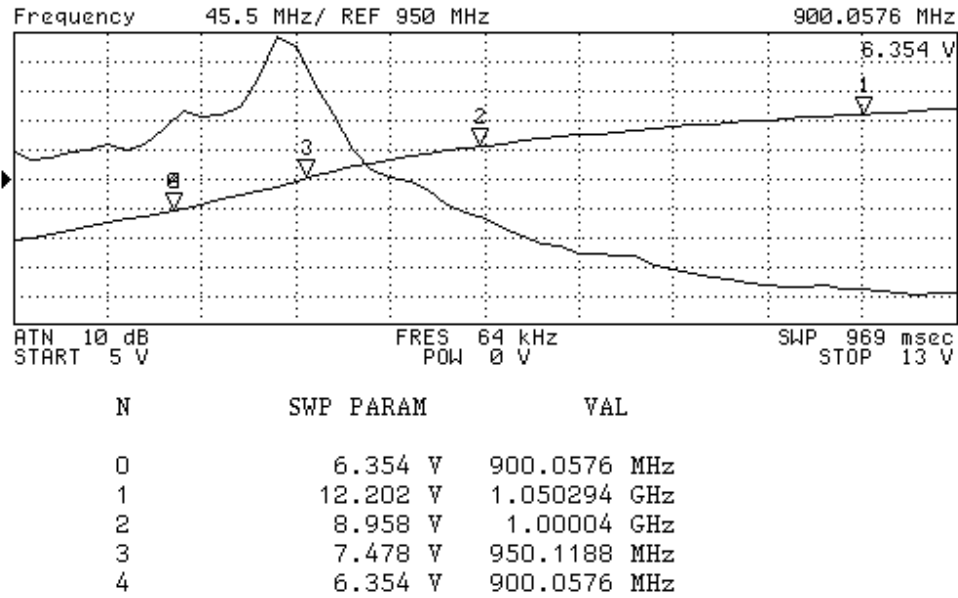


Figure 11 - Tuning Curve for Beta's VCO, Unloaded

As the graph shows, the tuning curve is increasing with an uneven slope and a voltage range of 6.4V to 8.9V is needed to obtain the 900MHz to 1GHz desired frequency range, which is an 40MHz/V gain constant using straight-line approximation. Note that this is higher than the 0.5V to 4.5V the VCO was desired for, which corresponds to a smaller varactor capacitance in the 3pF to 6pF range, as seen from the varactor datasheet. As the output of the VCO is the T-connector that creates the feedback tap and also a thru-path for the output to a spectrum analyzer or VCO meter. When loaded with this structure, the tuning curve changes to that seen in Figure 12, with a straight-line approximation gain constant of ~20 MHz/V.

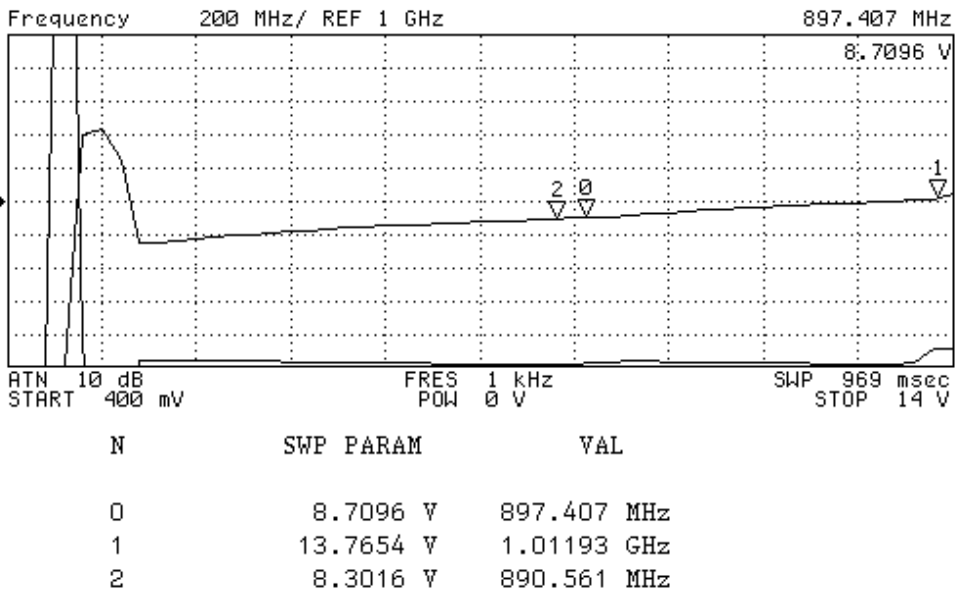


Figure 12 - Tuning Curve for Beta's VCO, Loaded with PLL board

Finally, a look at the output power vs control voltage in Figure 13 for Beta's unloaded VCO shows sufficient output power across a wide tuning range.

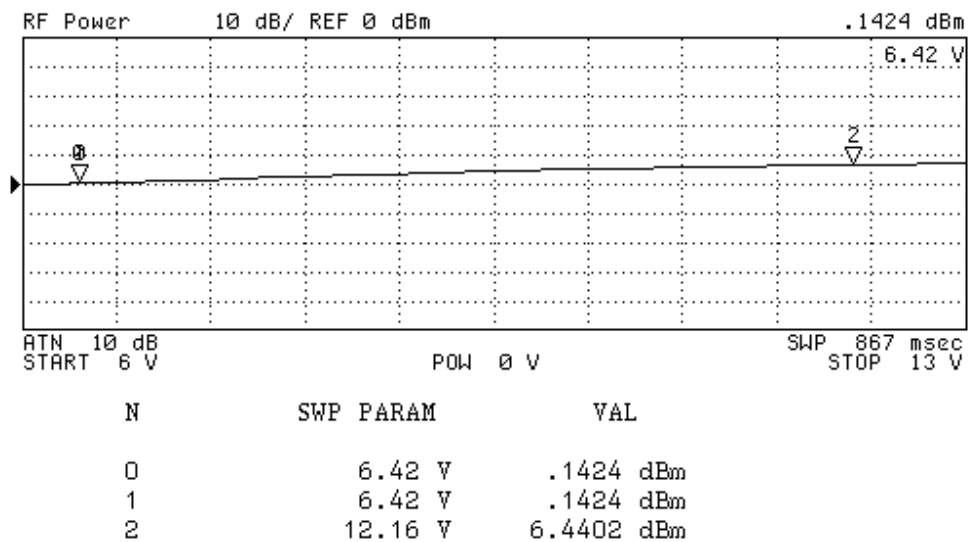


Figure 13 - Output Power vs Control Voltage, Beta's VCO, Unloaded

The characterization performed above was repeated for Alpha's VCO, whose physical construction is shown in Figure 14. It too places high importance in reducing parasitics by short path lengths. The collector here is tapped directly at the start, with the lead going just 2mm before contacting the ground plane. Chen used a thru-hole in order to position the 2SC3302 transistor in a more optimal orientation. An expansive ground plane surrounds the VCO structure.

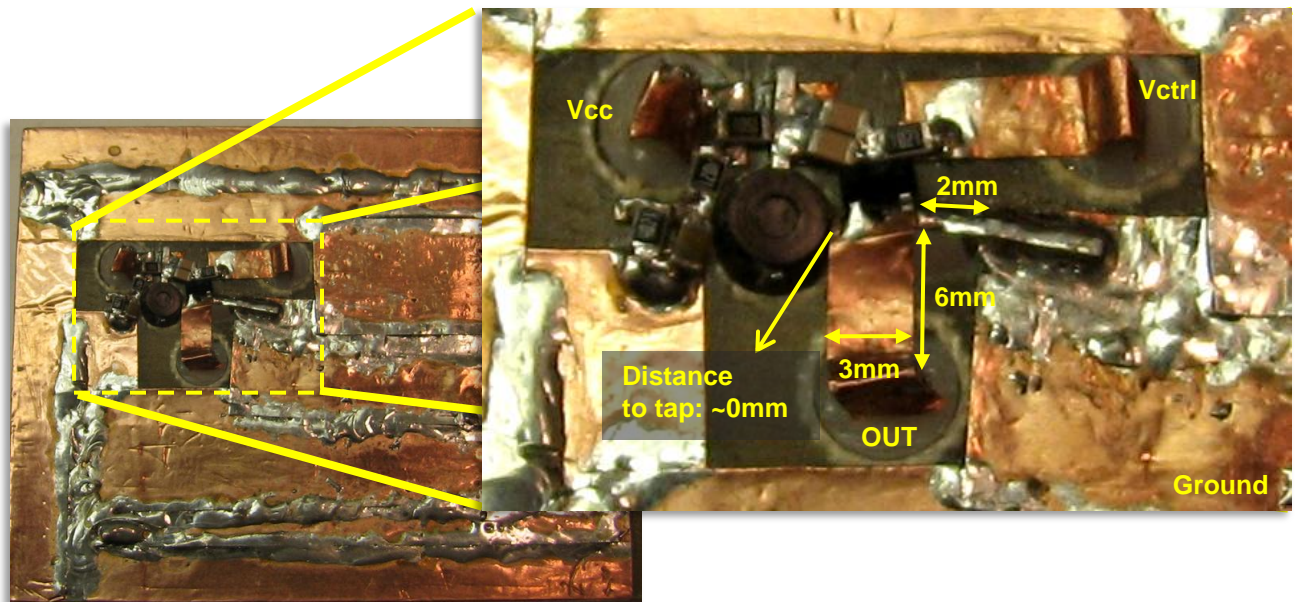


Figure 14 - Alpha's VCO with Entire Structure and VCO Close-Up

Tuning curves were measured for Alpha's board for the unloaded and loaded cases, shown in Figure 15 and Figure 16, respectively.

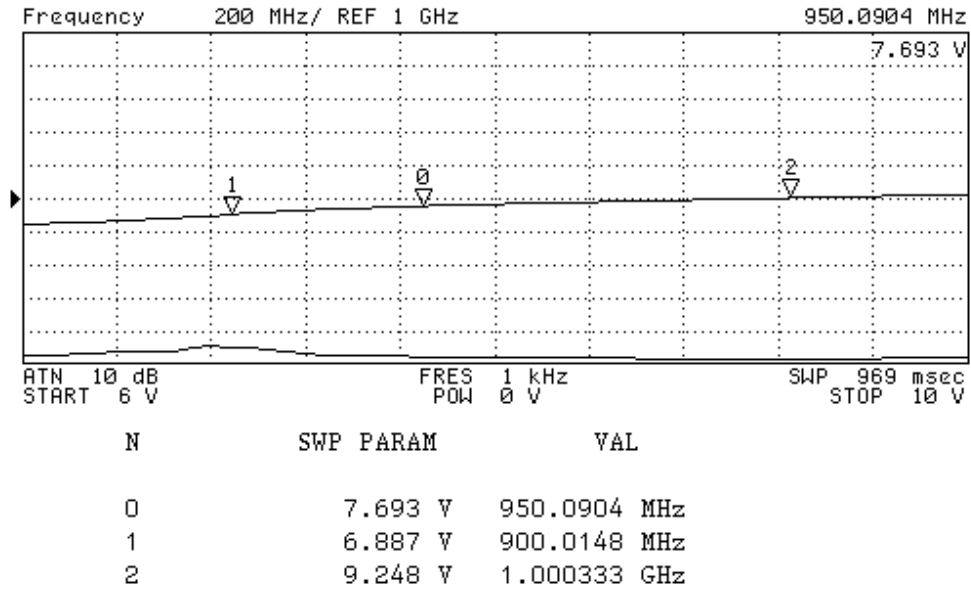


Figure 15 - Tuning Curve for Alpha's VCO, Unloaded

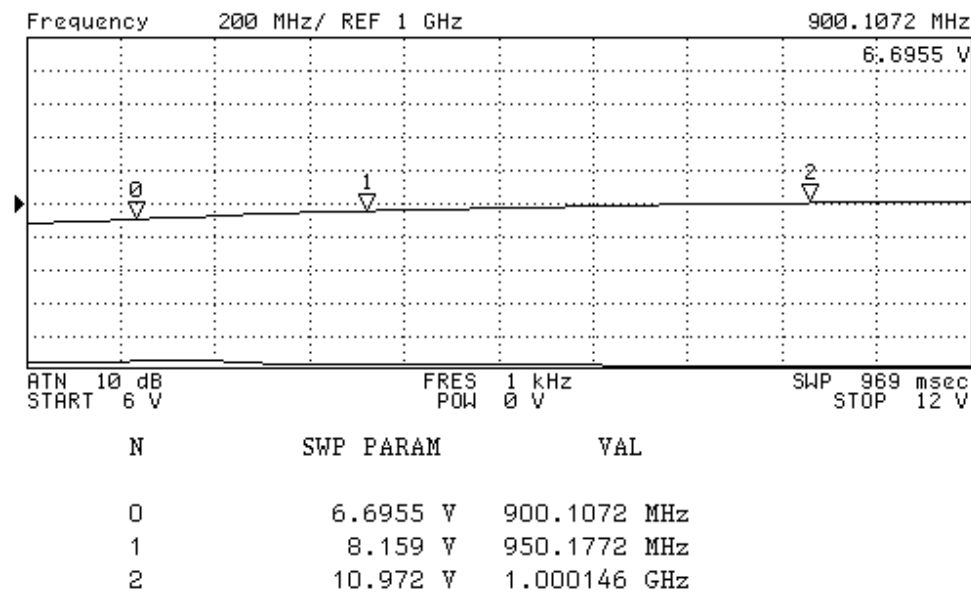


Figure 16 - Tuning Curve for Alpha's VCO, Loaded with PLL Board

Here the effect is again seen of voltage control spreading and corresponding reduction in gain constant when the VCO is loaded. The gain constant goes from 42MHz/V unloaded to 23.4MHz when loaded down. This further validates the assumption used for the PLL loop filter of gain constants between 20 and 25 MHz. Finally, the output power vs control voltage for Alpha's unloaded VCO is shown in Figure 17.

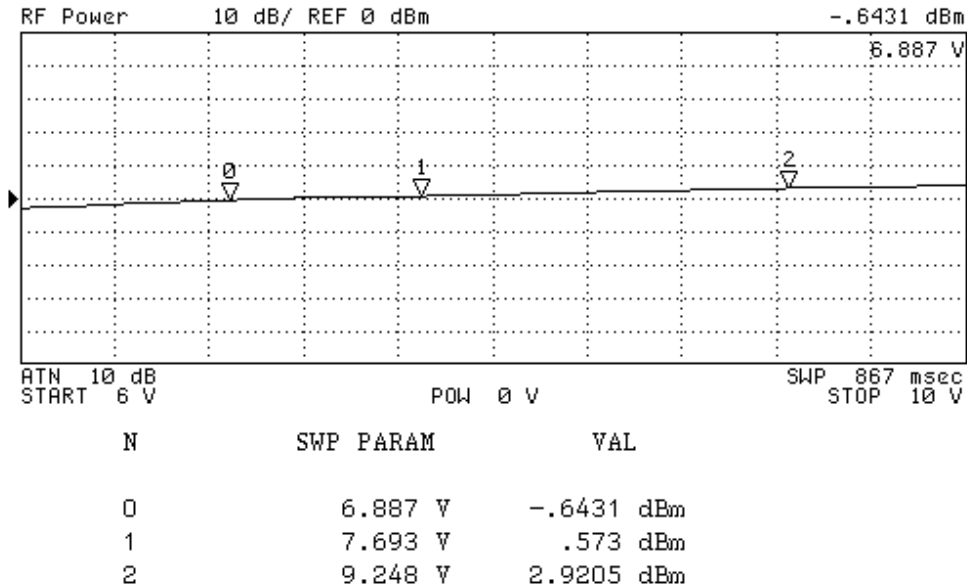


Figure 17 - Output Power vs Control Voltage for Alpha's VCO, Unloaded

Unlike Beta's VCO, this VCO shows lower output power and one that falls below the minimum of 0 dBm within the tuning range. Adjustments were made to the tapping, but the power could not be raised without sacrificing functionality.

Level Shifter

A significant challenge in building the oscillator was obtaining an inductance as small as 3 nH for the tank circuit while accommodating the innumerable inductive parasitics that were being contributed from almost all the elements that were placed on the board. After several attempts it was evident that to have a resonance frequency as high as 1 GHz the capacitance in the tank had to be reduced for which not only did we have to completely get rid of C_2 but also reduce the capacitance of the varactor by providing a control voltage that was much higher than PLL was generating. The datasheet of the MC12181 IC states that its output will be 0.5V to 4.5V for a 5V charge pump supply voltage, but our oscillator was needed a higher control voltage that ranged from ~6V to ~13.5V depending on loading to tune from 900MHz to 1GHz. Additionally, not only are the DC values higher than what the MC12181 can provide, the actual tuning range is not necessarily 4V. Furthermore, losses in the remaining loop filter stages could cause other changes in the control voltage that the VCO sees.

To provide the DC shift and to modify the tuning range, a summing operational amplifier circuit was used as shown in Figure 18.

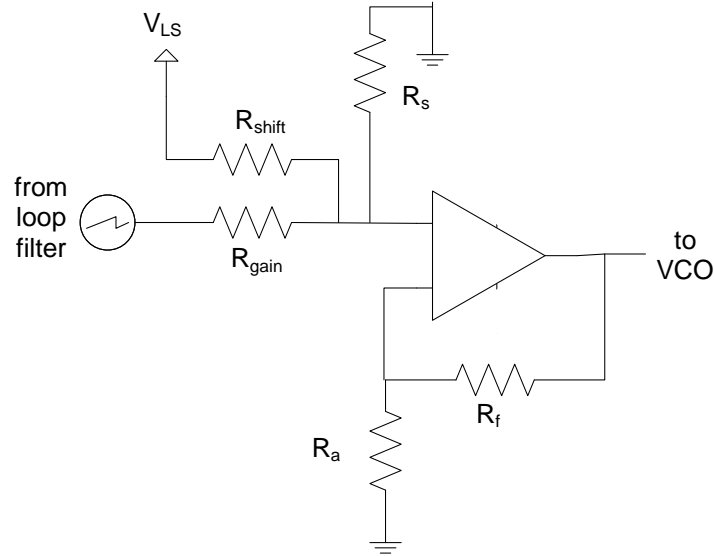


Figure 18 - Summing Amplifier Level Shifter

A dual op-amp IC (model NTE928M) was used for the single-supply op-amp block. The V_{LS} , or level shifter supply voltage, was used to both power the op-amp and provide the DC source that is scaled through the R_{shift} resistor. The following equations can be used to find the output voltage:

$$V_{out} = V_{LS} \frac{R_f}{R_{shift}} + V_{O,LF} \frac{R_f}{R_{gain}}, \text{ with } V_{O,LF} \text{ being the output voltage from the level shifter. The } R_s \text{ and } R_a$$

resistors are used to satisfy stability rules:
$$\frac{R_f}{R_s} = 1 + \left[\frac{R_f}{R_a} \right] - \left[\frac{R_f}{R_{gain}} + \frac{R_f}{R_{shift}} \right].$$

$R_f = R_s$ was arbitrarily chosen as 5k ohm and the remaining resistor values were designed for $V_{LS} = 13V$. $R_{shift} = 12.1k$ to obtain a DC shift of 5.38V, while the voltage range from the loop filter was increased by $\sim 1.5x$ by setting $R_{gain} = 3.3k$ ohm. This resulted in a $R_a = 2.61k$ ohm. Note that these values are for the Beta. The design methodology remained the same for the Alpha. The values for Alpha were for a $V_{LS} = 20V$, with $R_{shift} = 5k$ ohm and $R_a = 4.03k$ ohm.

As a final check, the Alpha and Beta VCOs were tested with a tuning voltage being fed into the level shifter. If the level shifter was properly functioning, the 900MHz to 1000MHz range should be comfortably attainable with an input of 0.5V to 4.5V. Figure 19 and Figure 20 show the tuning curves under this setup for the Alpha and Beta PLLs, respectively.

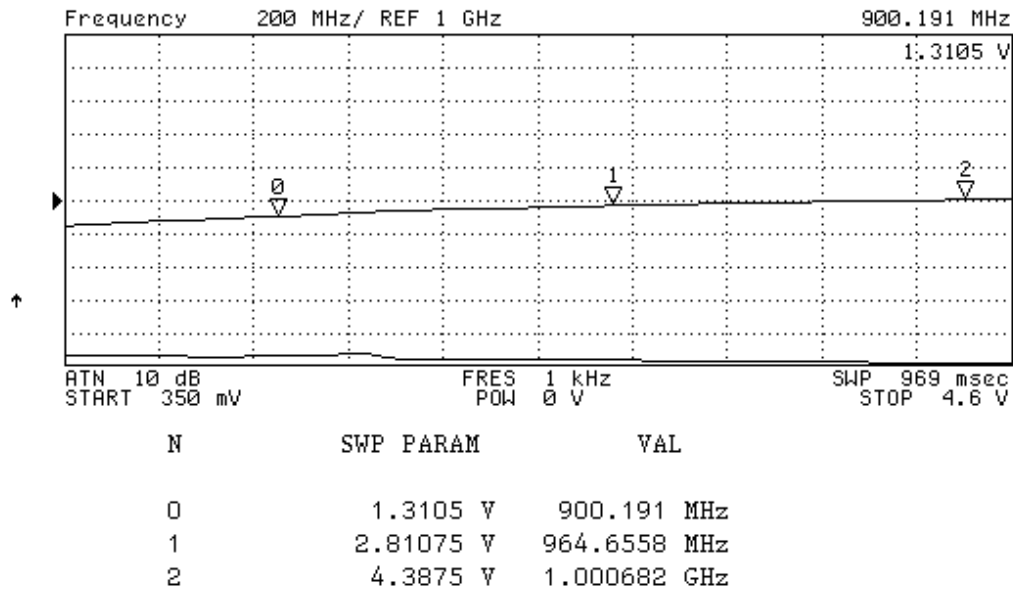


Figure 19 - Tuning Curve for Alpha's VCO with Level Shifter, Open Loop

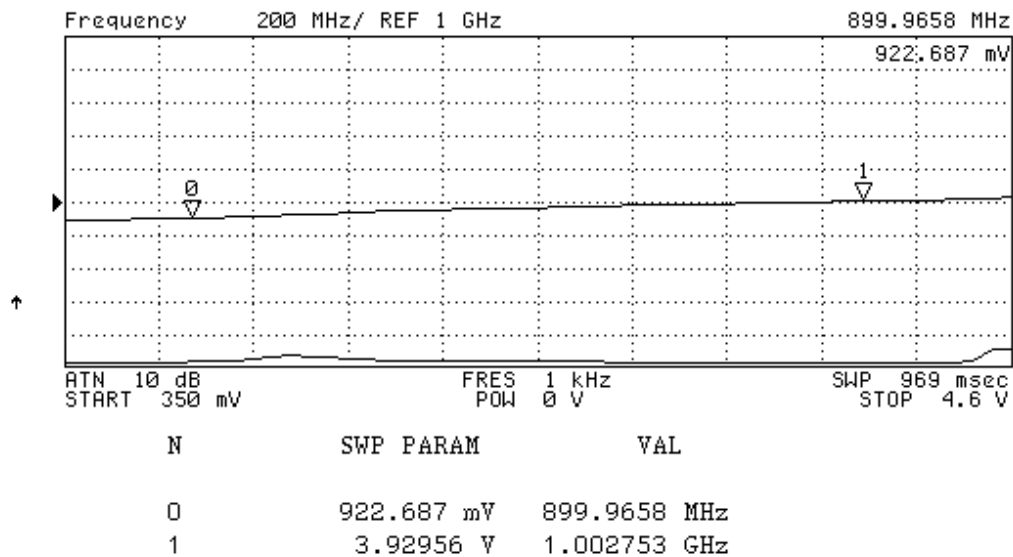


Figure 20 - Tuning Curve for Beta's VCO, with Level Shifter, Open Loop

Alpha needs a control voltage from loop filter between 1.31V and 4.38V while Beta requires 0.92V to 3.92V, both ranges that should be comfortably supplied by the MC12181. The gain constants, using straight-line approximation again, are 32.5MH/V and 33.5 MH/V, respectively.

Closing the Loop

The PLL entered closed-loop operation when the output of the loop filter was connected to the input to the level shifter. The output was observed on the spectrum analyzer. There were numerous obstacles in the journey towards obtaining lock at the desired frequencies.

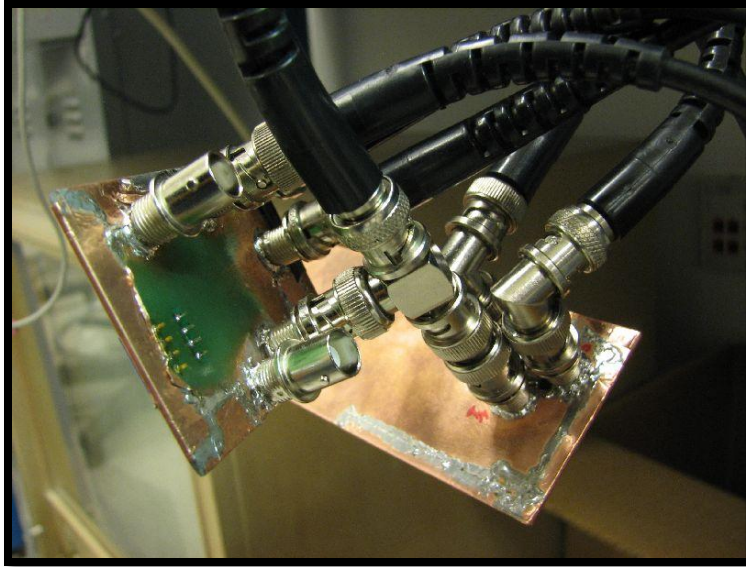


Figure 21 - Photo of the Closed Loop Setup

Figure 21 shows a picture of how the PLL board (on the left) connects with the VCO board (right side) through a T-connector. An early problem encountered was that the DIP switches that set the desired frequency seemed to have no effect on the output. V_{LS} (and thus the DC shift) was varied and the frequency output would shift, but the shape of the signal did not convey that a lock had occurred. An oscilloscope was used to probe various points with mixed results. We soon realized that the MC12181 chip was not consuming current so it was replaced.

The typical testing procedure involved setting the DIP switch to the desired frequency then adjusting V_{LS} such that a lock would occur. This was visually confirmed when the spectrum analyzer signal would become very distinct and the presence of side spurs could be clearly seen. The next desired frequency would be set and V_{LS} further changed to obtain lock. Proper PLL operation would have a single V_{LS} for all frequencies, so that all the user has to do is adjust the DIP switches to generate the desired frequencies. Despite many long hours analyzing the behavior of the level shift circuit, loading phenomenon, and replacing ICs, we were unable to achieve this. It was clear by documenting the output voltages from the loop filter and the level shifter for each of the frequencies that the act of closing the loop changed the tuning range of the VCO and thus made the previously designed level shifter no longer optimal. In order to mitigate this effect, a unity gain buffer between the loop filter and the level shifter was tried, utilizing the 2nd op-amp in the NTE928M IC. However, it is believed that this taxed the stability of the loop and would often cause hashing in the spectrum analyzer output, such as in Figure 22.

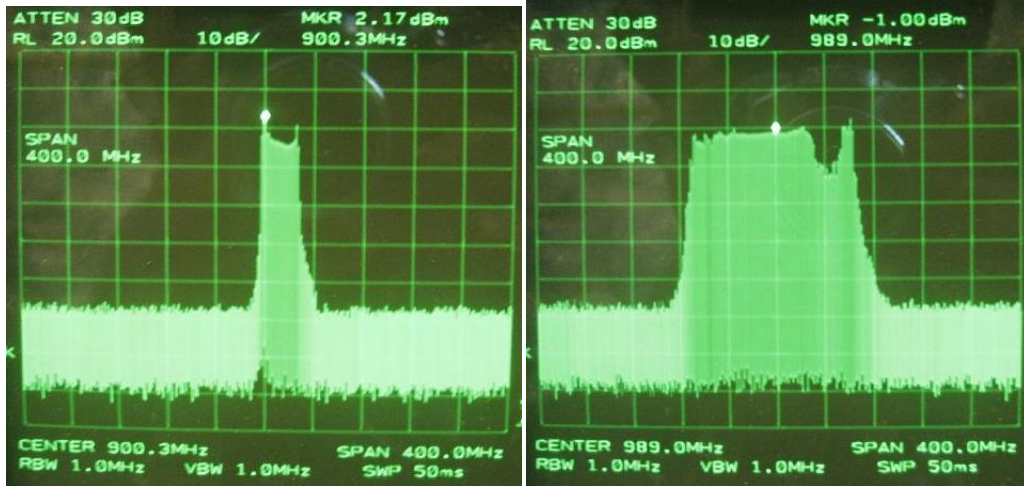


Figure 22 - Examples of unity gain buffer causing ‘hashing’ in spectrum

Some iterations saw that high or low frequencies could not be locked; the oscillator would only tune to a certain point. Adjusting the V_{LS} (ie, DC shift of the level shifter) extended this range. In other iterations, a lock could be obtained but it would be a loose one, with lots of shifting. Reflowing the solder joints usually rectified this problem, but it also motivated the change to a higher loop bandwidth, with us believing (erroneously or not) that the PLL would reduce this ‘seek’ time by speeding up the loop.

Despite the inability to operate from a single, constant V_{LS} , both Alpha and Beta PLLs were able to achieve a lock at all five frequencies of interest, albeit with differing characteristics. The measurements for both Alpha and Beta PLLs are discussed below.

Results

The Alpha PLL features excellent reference spur (f_{ref}) attenuation at all five frequencies of interest, approaching -60dBc in the case of the 1000MHz lock. However, while the output power at 975MHz and 1000MHz is quite good at 4.2dBm and 6.5dBm, respectively, the output power falls below 0dBm for the 925MHz and 900MHz frequencies. Table 23 shows the full measurements results, including phase noise measured at 100kHz and 1MHz offset from the carrier. These measurements were taken at a MC12181 supply voltage of 4.95V and a VCO supply voltage of -7.44V.

Alpha (Alpha’s VCO & Alpha’s board) Results

| Frequency (MHz) | Output Power (dBm) | f_{ref} Spur Attenuation (dBc) | Phase Noise 100 kHz Offset (dBc) | Phase Noise 1 MHz Offset (dBc) | V_{LS} Supply (V) |
|-----------------|--------------------|----------------------------------|----------------------------------|--------------------------------|---------------------|
| 900 | -5.0 | -43.3 | -83.0 | -116.4 | 14.1 |
| 925 | -2.5 | -45.7 | -74.8 | -104.5 | 14.9 |
| 950 | 1.5 | -45.7 | -85.4 | -120.9 | 17.4 |
| 975 | 4.2 | -51.3 | -86.4 | -120.9 | 19.2 |
| 1000 | 6.5 | -59.3 | -97.6 | -127.5 | 19.2 |

Table 23 - Results for Alpha

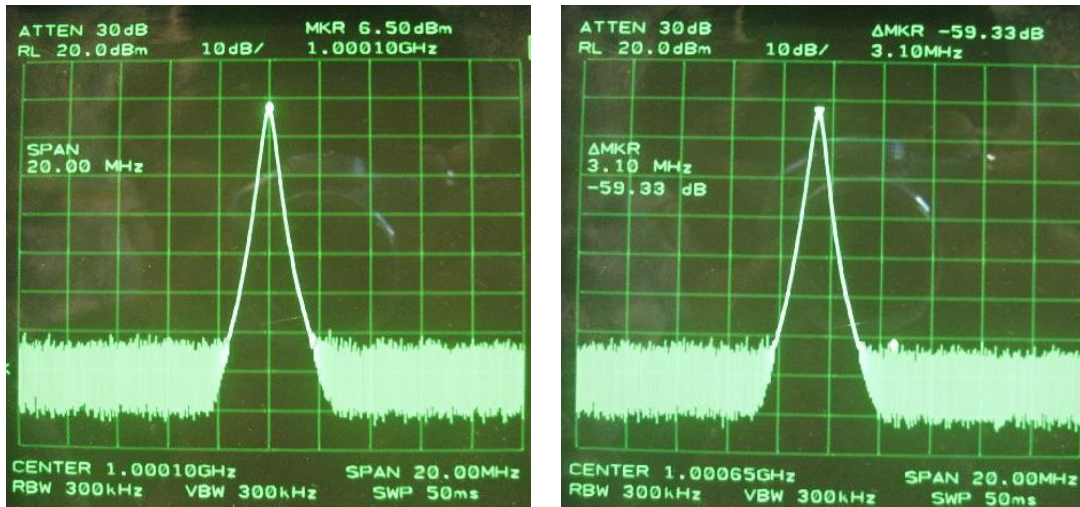


Figure 24 - Alpha's 1 GHz Lock, Output Power & Spur Attenuation

Figure 24 shows the spectrum analyzer for Alpha's 1000MHz lock. The left image shows the output power measured at the peak and the right image shows the difference between the power at the carrier and an offset of ~3.10 MHz, which corresponds to the reference spur. Figure 25 shows the phase noise measured with the VCO meter for the 1000MHz lock, averaged over 8 time periods. Spectrum analyzer images and phase noise measurements for the remaining four frequencies of interest can be found in Appendix A.

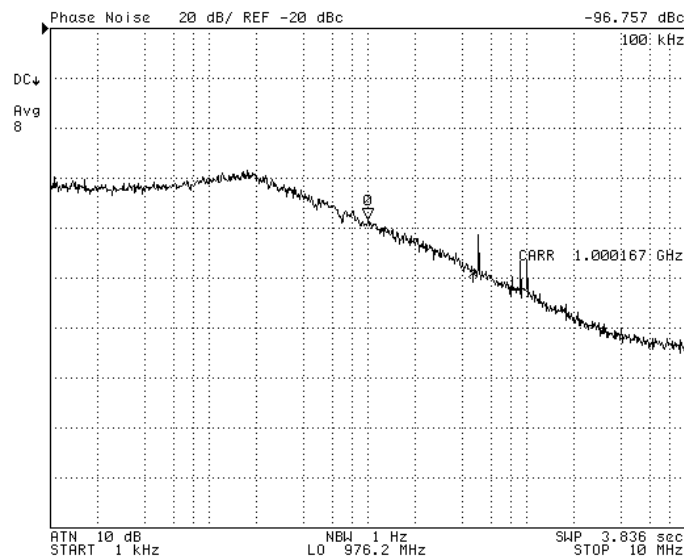


Figure 25 - Alpha's Phase Noise, 100 kHz offset from 1 GHz carrier

Finally, a summary of the minimum, nominal, and maximum gain constants for Alpha's VCO is shown in Table 26.

| Condition | Minimum (MHz/V) | Nominal (MHz/V) | Maximum (MHz/V) |
|-----------------------|-----------------|-----------------|-----------------|
| Unloaded | 32 | 42.2 | 61.7 |
| Loaded | 17.7 | 23.4 | 34 |
| Loaded w/ Level Shift | 22.9 | 32.4 | 43 |

Table 26 - Gain constant summary for Alpha

The Beta PLL provided more even performance across the frequency range. The measurements for Beta used a MC12181 supply voltage of 4.88V and a VCO supply voltage of -6.125V. The output power remained sufficient, ranging from 2.7dBm to 3.5dBm. The -30dBc spur attenuation specification was satisfied for all frequencies except 1000MHz, where the spurs were at -21.3dBc. Adjustments to the bias voltage and the V_{LS} did not reduce these spurs. Indeed, it is suspected that injected noise due to a layout issue at the root cause (or at least a contributor of several dB), because the orientation and contacting of the board caused changes to occur.

The Beta PLL took the brunt of the numerous iterating and debugging. After the spectrum analyzer images were taken, the phase noise measurements were about to begin when the voltage supply BNC connector to the Beta VCO broke off and took with it the resistors and capacitors used in the VCO. Time constraints did not permit a quick fix, so phase noise measurements for the Beta VCO are not included in this lab report. An addendum will be filed later that contains this data.

Beta (Beta's VCO & Board 2) Results

| Frequency (MHz) | Output Power (dBm) | f_{ref} Spur Attenuation (dBc) | Phase Noise 100 kHz Offset | Phase Noise 100 kHz Offset | V_{LS} Supply (V) | V_{OLF} (V) | V_{OLS} (V) |
|-----------------|--------------------|----------------------------------|----------------------------|----------------------------|---------------------|---------------|---------------|
| 900 | 2.7 | -38.5 | na | na | 10.8 | 2.89 | 8.8 |
| 925 | 2.7 | -31 | na | na | 11.1 | 3.34 | 9.6 |
| 950 | 3.2 | -34.9 | na | na | 12.6 | 3.63 | 10.57 |
| 975 | 3.5 | -40.7 | na | na | 14.7 | 4.02 | 11.67 |
| 1000 | 3.3 | -21.3 | na | na | 13.9 | 4.33 | 12.56 |

Table 27 - Results for Beta

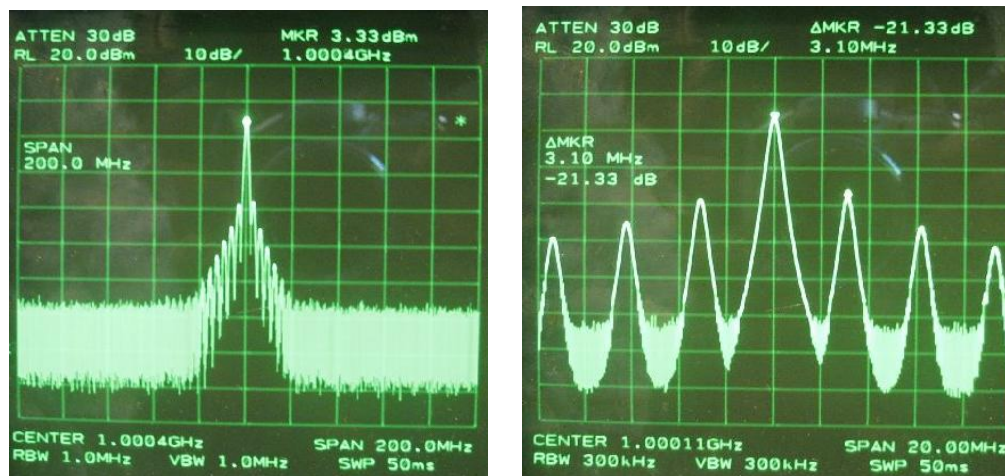


Figure 28 - Beta's 1 GHz Lock, Output Power & Spur Attenuation

As Figure 28 shows, the spur attenuation for Beta at 1000MHz is significantly worse than the Alpha board or any other frequency locked by Beta (full results shown in Appendix B). The left image also shows the characteristic shape on the spectrum analyzer while spanning a wide bandwidth (200MHz) when lock has been achieved. Table 29 summarizes the minimum, nominal, and maximum gain constants for different conditions for the VCO.

| Condition | Minimum (MHz/V) | Nominal (MHz/V) | Maximum (MHz/V) |
|-----------------------|-----------------|-----------------|-----------------|
| Unloaded | 33.8 | 38.2 | 44.2 |
| Loaded | ~17 | 21.2 | ~36 |
| Loaded w/ Level Shift | ~31.2 | 33.3 | ~36 |

Table 29 - Gain constant summary for Beta

Conclusion

This laboratory investigation lived up to its reputation as the most challenging assignment. The PLL is not a trivial block to understand and implement, and the voltage controlled oscillator is a whole task itself. Collaboration was key in constructing the VCO, particularly the result that parasitic and stray capacitances are sufficient to warrant the removal of C_2 all together in the Colpitts topology. For the PLL board, the most difficult element to implement was the level shifter. The nature of loading various components (the VCO, the loop filter, etc) resulted in an optimization design problem with a goal that was always moving.

Ultimately however, we were able to achieve lock at all frequencies of interest and met nearly all the specifications for each frequency too. We would have liked to have done so with a constant V_{LS} for indeed, this is what significant time was spent in trying to achieve.

Appendix A – Alpha Full Results for 900 MHz to 975 MHz Frequency Range

Output Power & Spur Attenuation

900 MHz:

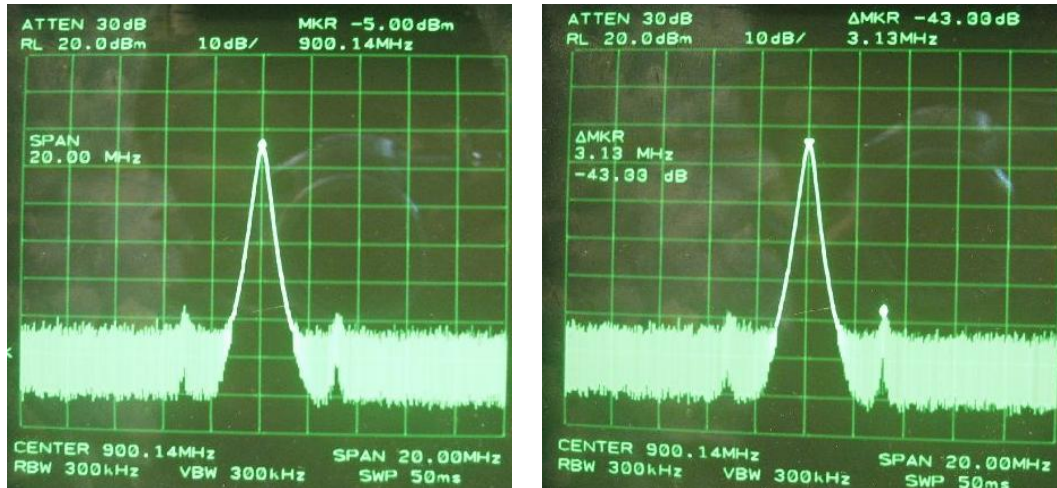


Figure 30 - Alpha's 900 MHz Lock, Output Power & Spur Attenuation

925 MHz:

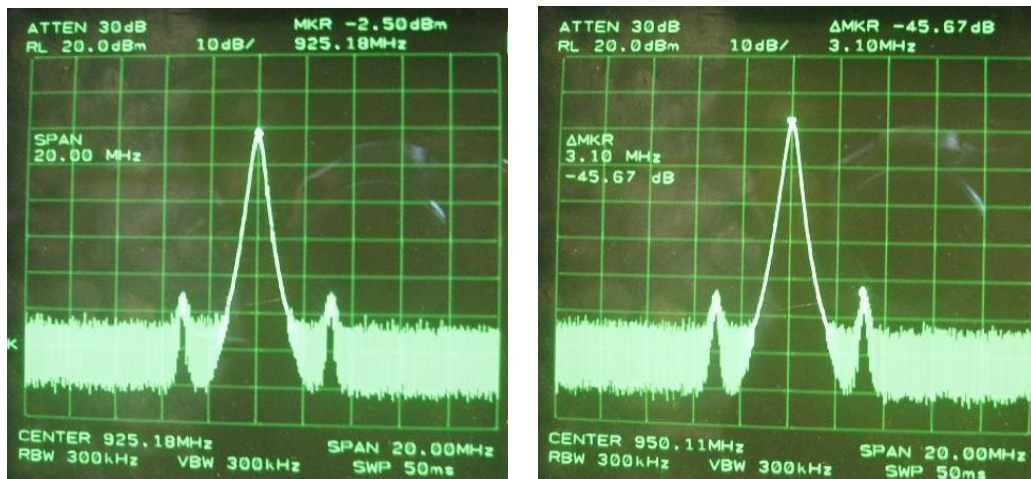


Figure 31 - Alpha's 925 MHz Lock, Output Power & Spur Attenuation

950 MHz:

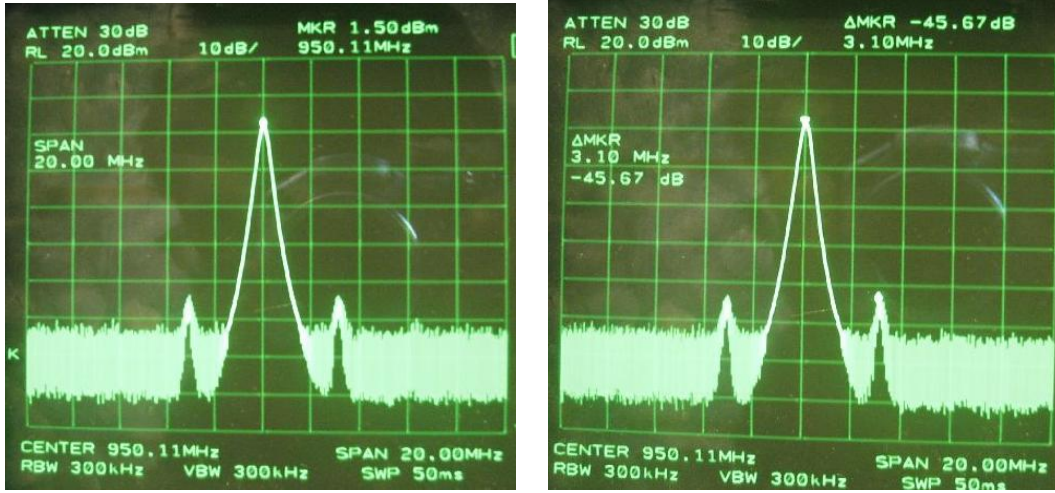


Figure 32 - Alpha's 950 MHz Lock, Output Power & Spur Attenuation

975 MHz:

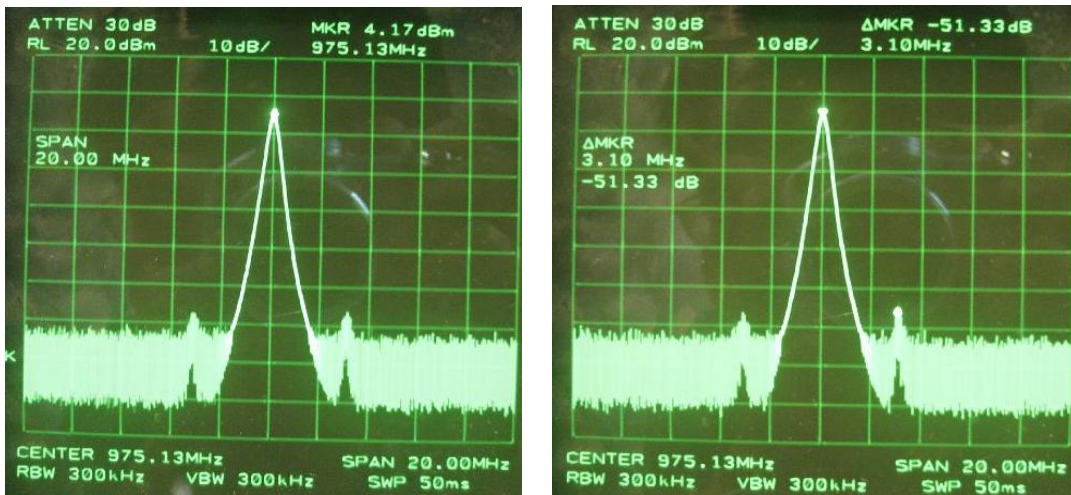


Figure 33 - Alpha's 975 MHz Lock, Output Power & Spur Attenuation

Phase Noise

900 MHz:

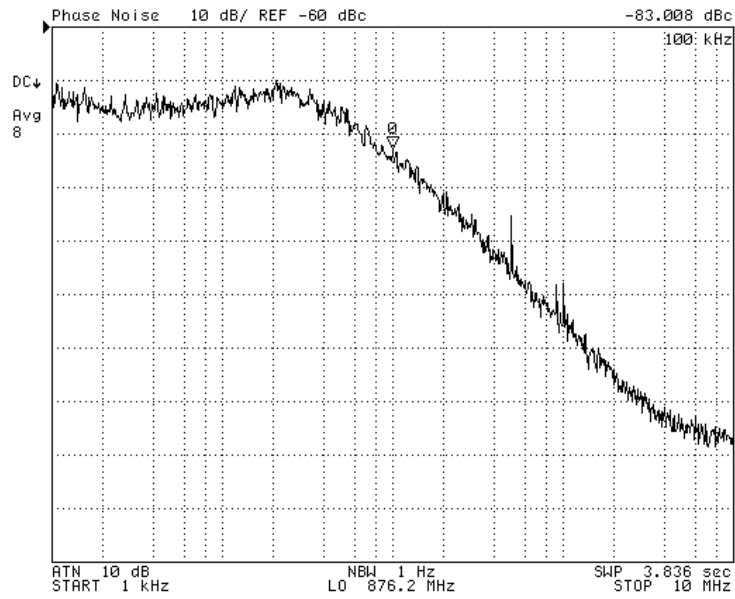


Figure 34 - Alpha's 900 MHz Lock, Phase Noise

925 MHz:

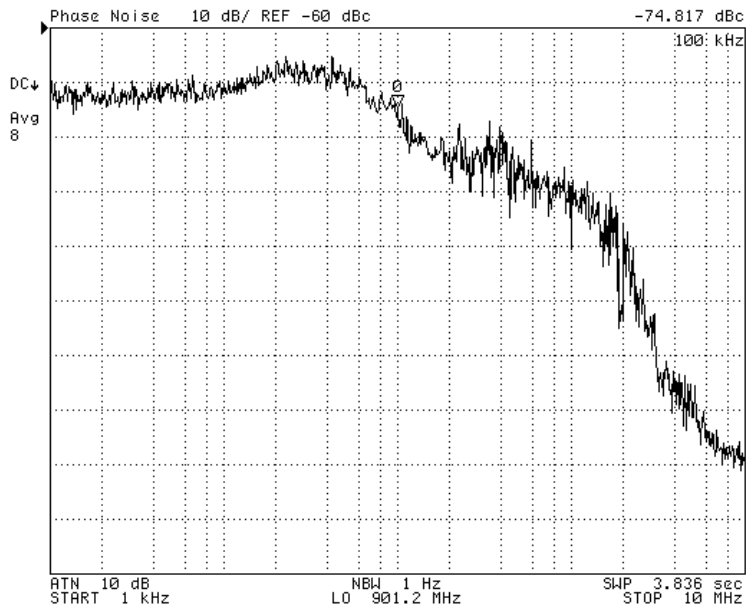


Figure 35 - Alpha's 925 MHz Lock, Phase Noise

950 MHz:



Figure 36 - Alpha's 950 MHz Lock, Phase Noise

975 MHz:



Figure 37 - Alpha's 975 MHz Lock, Phase Noise

Appendix B – Beta Full Results for 900 MHz to 975 MHz Frequency Range

Output Power & Spur Attenuation

900 MHz:

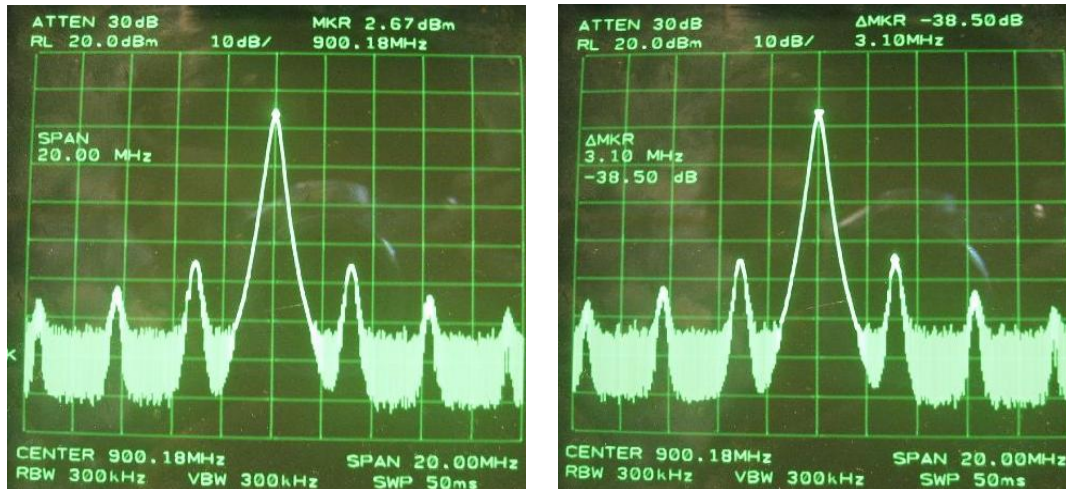


Figure 38 – Beta's 900 MHz Lock, Output Power & Spur Attenuation

925 MHz:

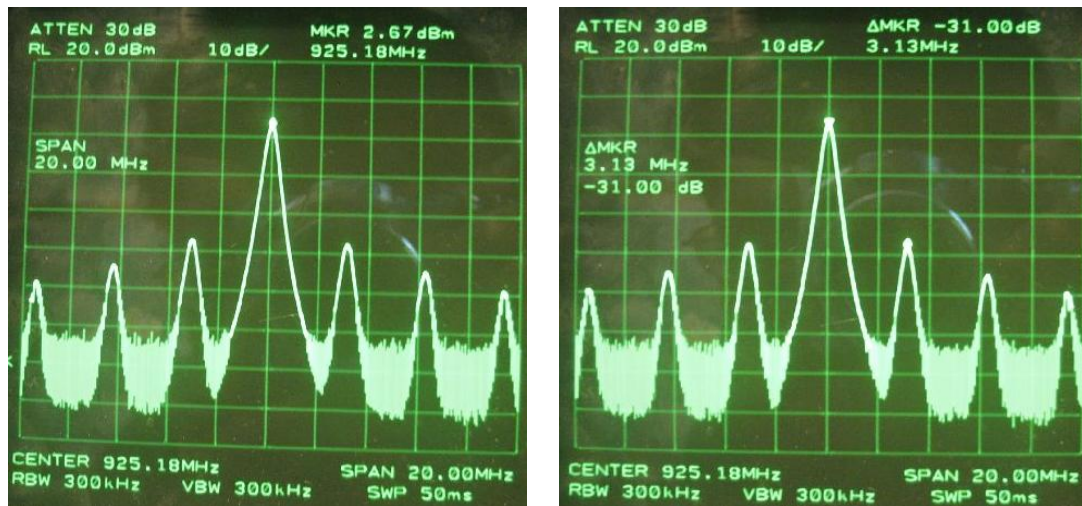


Figure 39 - Beta's 925 MHz Lock, Output Power & Spur Attenuation

950 MHz:

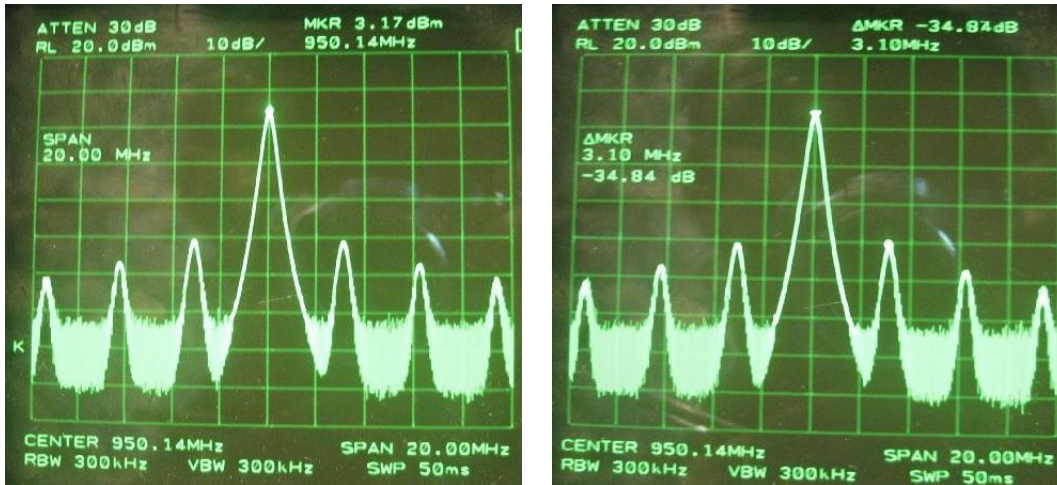


Figure 40 - Beta's 950 MHz Lock, Output Power & Spur Attenuation

975 MHz:

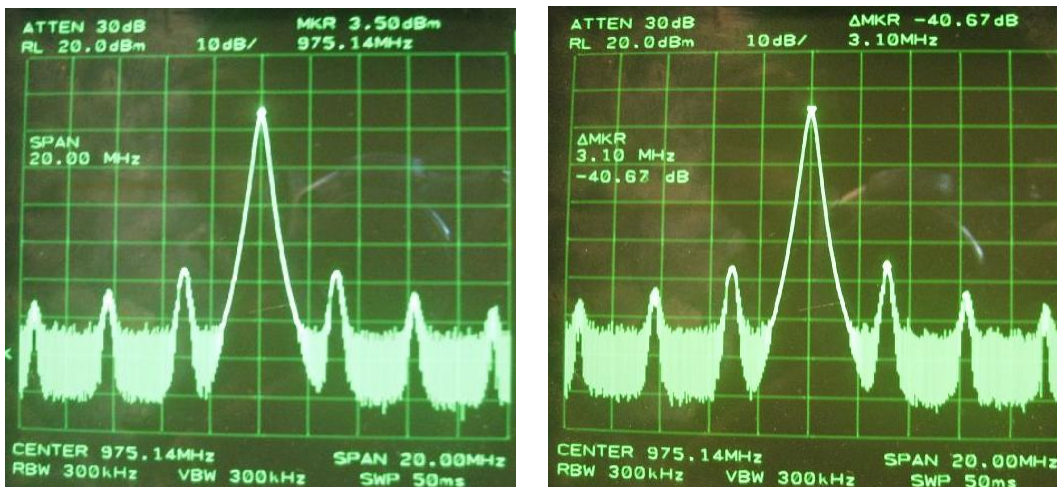


Figure 41 - Beta's 975 MHz Lock, Output Power & Spur Attenuation

Phase Noise

The Beta VCO board broke before phase noise measurements could be taken. The board will be prepared and phase noise measurements will be submitted as an addendum.

Appendix C – Loading Characterization of the VCO

The output of the VCO first goes through a BNC connector, then a T-connector to which the BNC-input to the F_{in} is connected and the cable to the spectrum analyzer or the noise meter. This total loading structure was characterized on the VNA for both Chen and Beta's board, shown below:

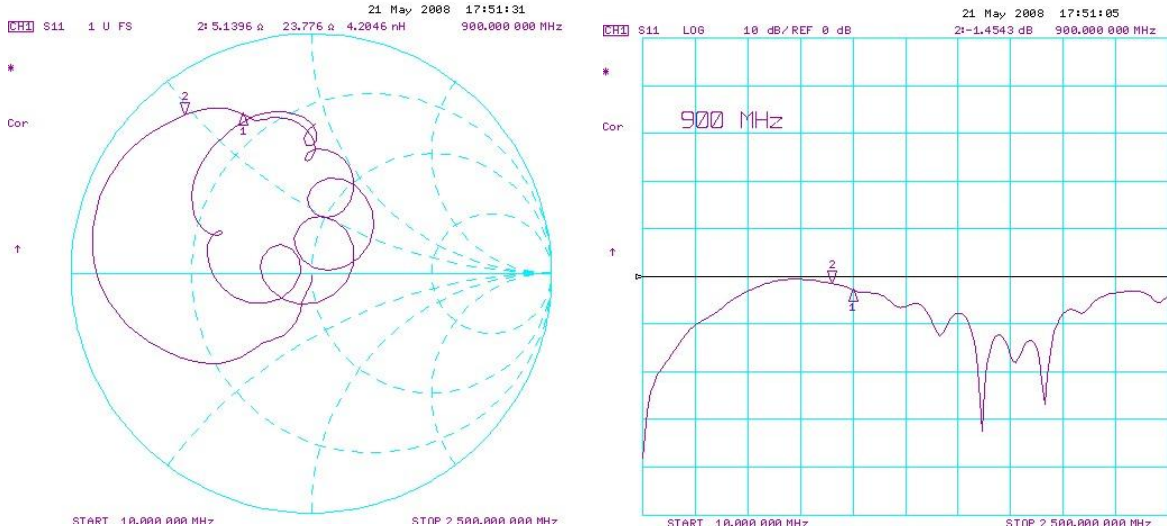


Figure 42 - S₁₁ of VCO's Load using Alpha's VCO & Board in Smith Chart & Log Magnitude

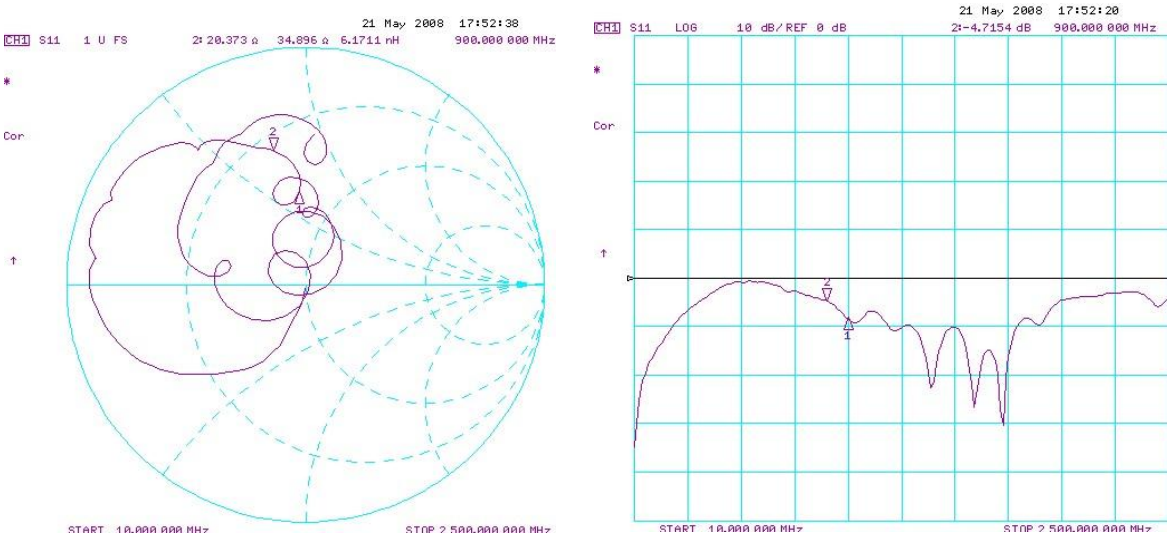


Figure 43 - S₁₁ Looking into VCO's Load, Beta's VCO & Board, Smith Chart & Log Magnitude

| Board & Frequency | | Smith Chart | Log Magnitude |
|-------------------|----------|--------------|---------------|
| Chen | 900 MHz | 20.4 + j34.9 | -4.7 dB |
| | 1000 MHz | 35.1 + j31.9 | -8.3dB |
| Panwar | 900 MHz | 5.14 + j23.8 | -1.45 dB |
| | 1000 MHz | 11.3 + j31.7 | -2.8dB |

Figure 44 - Loading Seen by the VCOs