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May 8, 2006

TO: Dr. Tom Conte
FROM: Saket Vora
SUBJECT: ECE 492G – Independent Research Study – Final Report

Dr. Conte,

This report contains the bulk of my research for this semester. First, I would like to re-iterate my thanks and appreciation for agreeing to advise me for this independent research study course on relatively short notice. It has given me an opportunity to meet more faculty members, explore an area that few people have trodden, and has increased my theoretical and practical knowledge regarding signal processing.

This project began in exploring the rapidly rising field of field-programmable analog arrays. Research into this field showed the low power benefits of analog signal processing and the ways that analog techniques could drastically simplify computationally intensive operations in a microprocessor. The unique approach of this project was to start from the digital mindset of an embedded systems designer and work backgrounds from the digital filter to the analog filter. I first realized the novelty of this approach when I began speaking with graduate students and professors knowledgeable in this area – it was something they had not quite thought of doing. A possible application for this framework was in a low power MP3 encoder, and time was spent in researching the MP3 algorithm and encoding characteristics. However, as the big picture was further discussed, a much more fundamental challenge to this project came into light: how does one go from the *z*-plane to the *s*-plane and still maintain stability and the desired frequency response characteristics? Answering this question ultimately became the main thrust of this research effort.

In surveying the current literature on the topic, numerous resources discuss ways of going from the *s*-plane to the *z*-plane by using the bilinear transform, for example. I searched the IEEE Xplore database for papers relating to analog signal processing, analog FIR filter implementations, and FPAA architectures in general. In studying these works, the analog implementation benefits became clearer, yet the nagging issue of the existing work using quantized time (sample-data waveforms from sample-and-hold circuits) remained. Because of the switched-capacitor basis for FPAAs (such as Anadigm's chips), the focus was shifted instead to programmable biquads on the recommendation of Dr. Griff Bilbro. These biquads were active RC filters with standardized topologies that could be configured to implement key filter specifications.

In order to test a conversion process, a 4-tap FIR filter was chosen as a test filter. MATLAB was used heavily to calculate the FIR filter coefficients, plot the frequency responses and zero-pole plots, and perform the *s*-plane to *z*-plane transformations. My proficiency with MATLAB greatly increased over the course of this research project. Through much experimentation and theoretical scratchwork in a journal, a methodology for implementing an analog *s*-plane filter that closely mimics the digital filter's frequency response was achieved, namely in matching the dc-gain and the cut-off frequency. The process and results of this method is shown in this report. I will admit that the mathematics of all the Laplace and *z* transforms, the Nyquist criteria, and filter characteristics overwhelmed me at times. Every week as I sat down to work on this project (I devoted my Tuesdays and Thursdays for this), I often ran through a quick review of the accumulated material in order to keep everything straight.

Future and more thorough investigations of this topic would involve testing the validity of this process for filters with higher sampling rates, cut-off frequencies, or more complicated topologies than a FIR filter. In addition, the steps for expressing the *s*-plane transfer function in a quantized, standardized form and actually implementing a physical programmable biquad still need to be worked out and explored.

I plan on presenting a summarized version of this research project at next year's Undergraduate Research Symposium. This year's deadline occurred too soon for me to have quality results. Thank you again for mentoring me with this challenging, interesting, and exciting project. Please contact me at any time if you have further questions.

Sincerely,
Saket Vora

Process for a Programmable Analog Adaptive Filter from Digital Tap Coefficients

By Saket Vora

Abstract— This paper presents a process for programming a truly continuous time analog adaptive filter beginning with digital tap coefficients, such as those used in digital signal processing methods. The motivation is to enable embedded systems to, in essence, 'compile' code written for a DSP framework and implement it in an analog filter design, thereby decreasing the power consumption of the filtering process. The method used in the proposed process involves mapping the digital filter's poles and zeros in the *z*-plane to an ideal analog filter's *s*-plane and ensuring an acceptable frequency response. A programmable bi-quad is proposed for implementing the analog filter.

***Index Terms*— analog signal processing, *z*-plane to *s*-plane mapping, tap coefficients, embedded systems filtering**

I. INTRODUCTION

FOR years digital filters have dominated the field of signal processing due to their high degree of programmability and maintaining accuracy. Analog filters were time-consuming to design and fabricate while offering almost no re-programmability. In addition, process variations and non-ideal physical environments would degrade their accuracy. However, modern processes have improved significantly to make analog circuits robust and able to maintain approximately 10 bits of accuracy. Techniques such as programmable bi-quads and recently field programmable analog arrays have introduced the idea of practical re-programmability to analog circuits and filters [1-7].

With the greater emphasis on improving the longevity of portable electronics, low power consumption is becoming increasingly more important. Analog filters can feature dramatically improved power consumption characteristics compared to their digital peers because operations that require repeated intensive computation by the digital signal processor are not required in an analog setting[2]. In [8]-[10], methods are discussed in implementing FIR filters using analog techniques.

Switched-capacitors have been a preferred method for implementing FPAAs and features good accuracy. However, switched-capacitor circuits have higher noise and offset voltage than passive or active filters[11]. In addition, they are analog in magnitude and quantized in time, due to the sample-and-hold method utilized. This sampled-data signal allows switched-capacitor based FPAAs to utilize a digital filtering mindset, with *z*-transforms and delays. Multiple clock lines at different frequencies are required for such an FPAA, and the many switches degrade performance[1].

True continuous time transfer functions are realized from the poles and zeros on the *s*-plane. In converting an existing digital filter, one method is to begin with the desired analog specifications and design the filter using standardized active filter topologies and transfer functions. Once an s-plane transfer function is determined it can be realized with, for instance, a programmable biquad[6]. However, this case-by-case conversion process in impractical when quick re-programmability is required or in a high speed adaptive filtering implementation.

II. Proposed Process for Determining Analog Transfer Function

A. *Process Outline*

A process is proposed that will take a digital filter (such as a FIR filter, in this case) in the form of its tap coefficients and calculate the analog s-plane transfer function. This transfer function, when expressed in a quantized and standardized topology, can then be implemented using a programmable biquad. There are numerous standardized active RC filter topologies for low pass, high pass, band pass, and band stop filters. A bank of resistors and capacitors with a cross-bar network interface with the biquad's amplifiers would be available to physically implement the s-domain transfer function. The microprocessor would send digital words to the biquad that when decoded would close the appropriate crossbar switches necessary to implement the determined transfer function with the proper topology. Because a crossbar connected bank of resistors and capacitors can provide a discrete number of possible values, the ideal zero and pole locations will have to be quantized to what the programmable biquad can physically implement.

Such a process would allow embedded system designers to continue to work in a digital mindset but ultimately realize the low-power benefits of analog signal processing. In an adaptive setting, the output of the analog filter would be sampled with an A/D converter and checked by the microprocessor for desirable characteristics. If an adjustment is required, such as the appearance of high frequency noise that must be attenuated, the microprocessor will compute new tap coefficients. These updated coefficients are converted through the process then downloaded to the analog filter. Figure 1 depicts a flow chart for the proposed process.

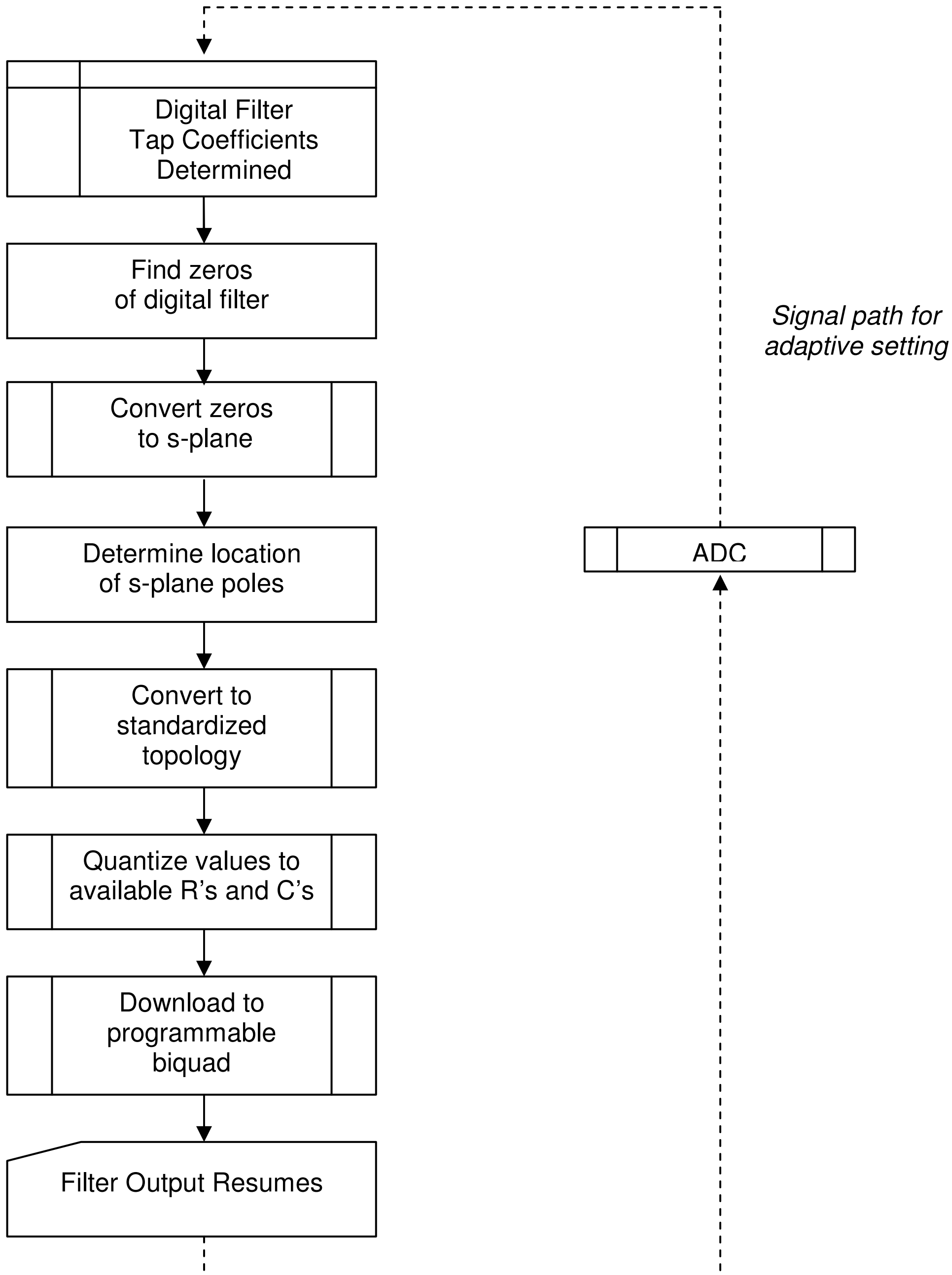

Figure 1 – Process flow chart

At the core of the conversion process, poles and zeros in the z-plane of the digital filter must be mapped onto the *s*-plane for the analog filter. Discussion of *s*-plane to *z*-plane mapping can be found in nearly every signal processing textbook. Mapping in the other direction, however, is not. The first part of this research endeavor involved studying the relationship between the *z*-

plane and the *s*-plane.

Applying a Laplace transform to a signal sampled at *T* is shown below [12] :

$$X^*(s) = \sum_{k=0}^{\infty} x(kT)\, e^{-kTs}$$

Substituting $z = e^{sT}$ results in the definition of the one-sided *z*-transform.

$$X(z) = \sum_{k=0}^{\infty} x(k)\, z^{-k}$$

The exact relationship between the complex variables *s* and *z* is $s = \frac{1}{T}\ln(z)$.

The conformal mappings of the *s*-plane to the *z*-plane and vice-versa were plotted using this relationship using MATLAB. An array of points in each plane was taken and transformed. The mapping was colorized to aid in depicting where the transformed points lie on the complementary plane. A sampling frequency ω_s of 8 rad/sec was used.

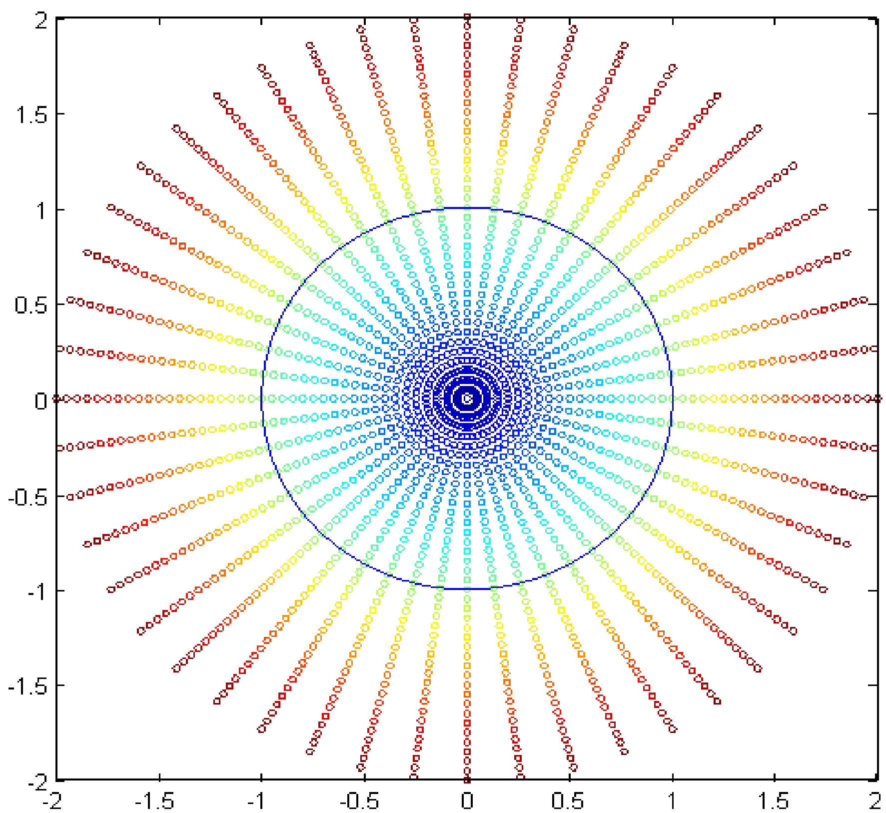

Figure 2 – A radial distribution of points on the *z*-plane. The unit circle is denoted with the blue line.

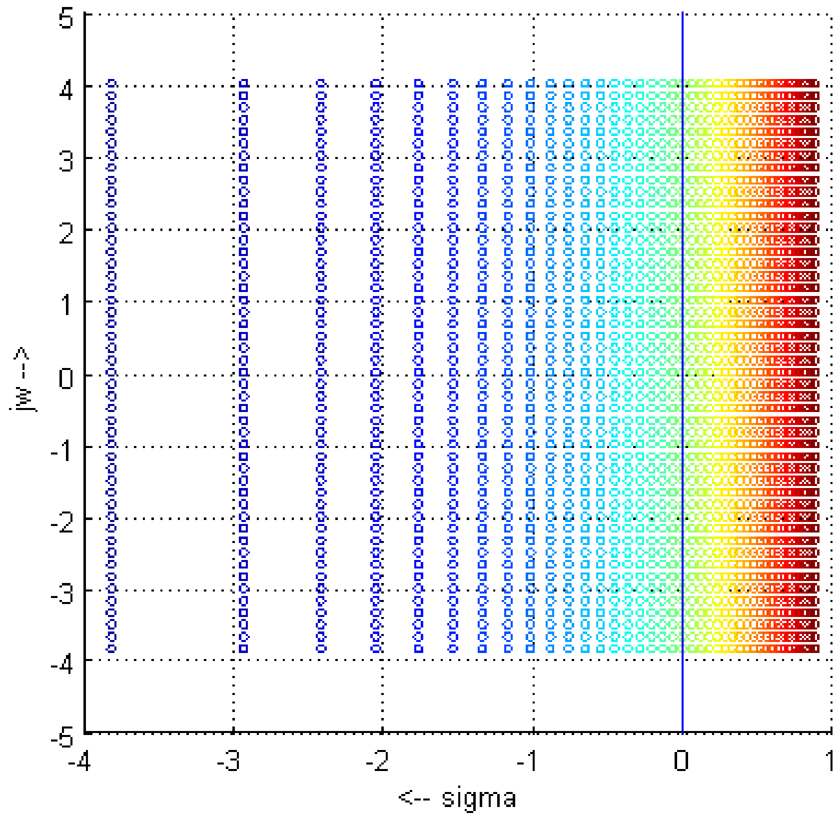

Figure 3 – The *z*-plane points in Figure 2 mapped onto the *s*-plane. The *jω*-axis is denoted with the blue line.

This mapping is consistent with the known stability characteristics of the *z*-plane and the *s*-plane. A discrete-time impulse response is stable if all its poles are located inside the unit circle in the *z*-plane. A continuous-time impulse response if all its poles are located in the left half of the *s*-plane, or has a real component of less than 0. The yellow and red points in Figure 2 map to the right half side of the *s*-plane, and the cyan and blue points in Figure 2 map to the left half side of the s-plane. Also, the mapping on the *s*-plane extends to ±*j*4. Because of the sampling, the points on the unit circle with an angle of ±π translate to $\pm j\frac{\omega_s}{2}$. This satisfies the Nyquist criteria for sampling.

Using this knowledge of *z*-plane to *s*-plane mapping, an example conversion is demonstrated with a digital filter.

III. EXAMPLE TRANSFORMATION: 4-TAP FIR FILTER

To demonstrate the transformation process of a digital filter to an analog filter, a 4-tap (third-order) FIR filter was designed with a specified cut-off frequency of 1.25 rad/sec. A FIR filter has the following transfer function:

$H(z) = \dfrac{a_0 z^3 + a_1 z^2 + a_2 z + a_3}{z^3}$, or alternatively $H(z) = a_0 + a_1 z^{-1} + a_2 z^{-2} + a_3 z^{-3}$.

The tap-coefficients for this filter are a_0, a_1, a_2, and a_3. MATLAB was used to generate the coefficients for this low-pass FIR filter using the `fir1(n,Wn)` command, with n being the order and W_n being the normalized cut-off frequency. The tap coefficients were $[a_0\ a_1\ a_2\ a_3]$ = [0.0449 0.4551 0.4551 0.0449]. A zero-pole plot of the z-plane and frequency response of the FIR filter is shown below.

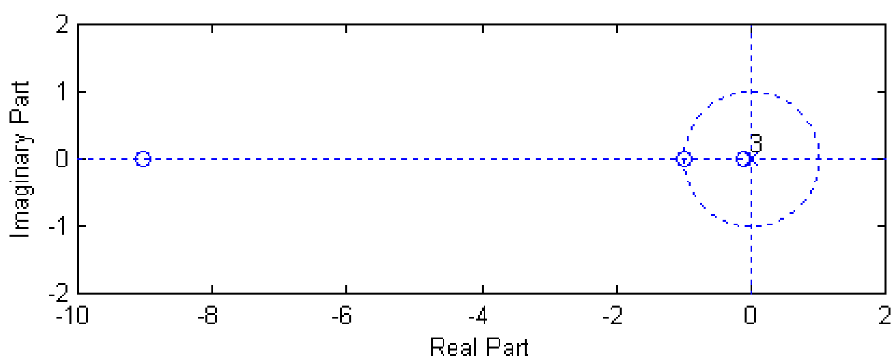

Figure 4 – A zero-pole plot of the FIR filter in the *z*-plane.

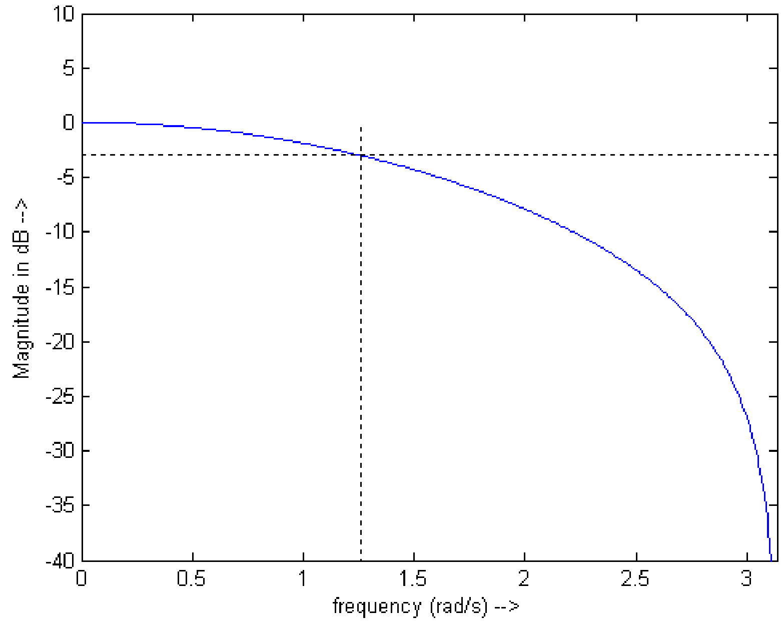

Figure 5 – Frequency response of the FIR filter.
The -3.01 dB and cut-off frequency denoted with dashed lines.

The zeros of the FIR filter were mapped onto the s-plane using the $s = \frac{1}{T}\ln(z)$ relationship described in section II, for a sampling frequency of 8 rad/sec. A FIR filter is always causal, for all of its poles lie at the origin of the *z*-plane. This presents an interesting transformation problem, because the origin of the *z*-plane is mapped to the negative infinity on the real axis of the *s*-plane. Not only is such a pole location impractical to physically implement, it alters the magnitude of the *s*-plane analog frequency response. The magnitude of the frequency response is $\left|H(j\omega)\right| = \frac{\prod z_{vectors}}{\prod p_{vectors}}$, where $z_{vectors}$ is the product of the vectors from each zero to the $j\omega$-axis and $p_{vectors}$ is the product of the vectors from each pole to the $j\omega$-axis for a given ω. If the poles are located at negative infinity on the real axis, then the magnitude response would approach 0 for all ω. The *s*-plane zeros are shown in the figure below.

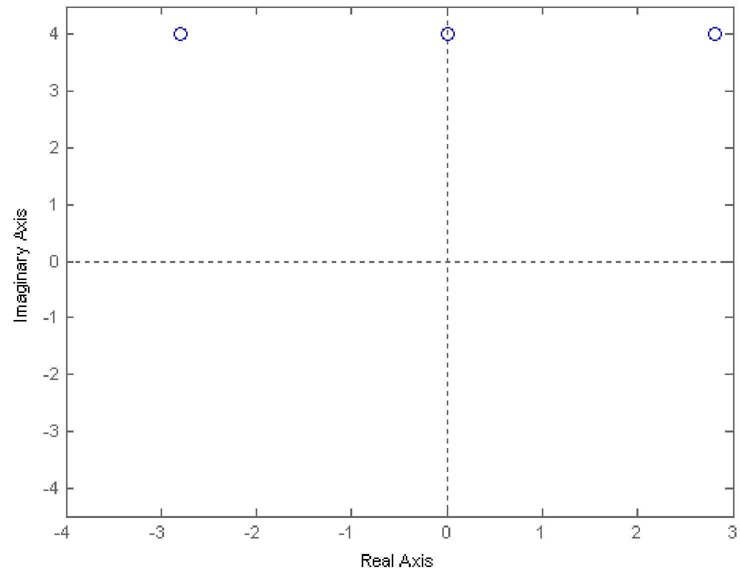

Figure 6 – Plot of the mapped zeros on the *s*-plane.

An optimal location for the poles can be determined using the location of the *s*-plane zeros, the desired cut-off frequency, and the dc magnitude of the frequency response.

The cut-off frequency is that frequency at which the magnitude decreases by approximately, 3.01dB, which is 0.7071 in pure magnitude. For the example filter, $|H(j1.25)| = \frac{\prod z_{vectors}}{\prod p_{vectors}} = 0.7071$.

The mapped zeros are located at $\pm 2.8 + j4$ and $j4$.

$$|H(j1.25)| = \frac{\left(\sqrt{2.8^2 + (2.75)^2}\right)^2 \cdot 2.75}{\prod p_{vectors}} = \frac{42.3569}{\prod p_{vectors}} = 0.7071$$

$$\prod p_{vectors} = \frac{42.3569}{0.7071} = 59.8997$$

All poles will be located at the same location, thus each pole vector is equivalent. The length of the pole vector from the $j1.25$ point is then $p_{vector} = \sqrt[3]{59.8997} = 3.91268$. Thus, in order to meet the desired cut-off frequency, the location of the poles must lie on a circle with radius 3.91268 with center point $j1.25$.

The digital filter's frequency response had a dc magnitude of 0 dB, which is 1 in pure magnitude.

$$|H(j0)| = \frac{\prod z_{vectors}}{\prod p_{vectors}} = \frac{\left(\sqrt{2.8^2 + 4^2}\right)^2 \cdot 4}{\prod p_{vectors}} = \frac{95.36}{\prod p_{vectors}} = 1 \;\therefore\; \prod p_{vectors} = 95.36$$

When all the poles are located at the same point, the length of the pole vector is $p_{vector} = \sqrt[3]{95.36} = 4.569$. In order for the dc magnitude of the analog filter to be 1, the pole vector must be at a radius of 4.569 from the origin.

These two conditions, the cut-off frequency and the dc gain, each define a circle on the *s*-plane. The point that satisfies both conditions is where the two circles intersect. Figure 7 depicts these conditions graphically.

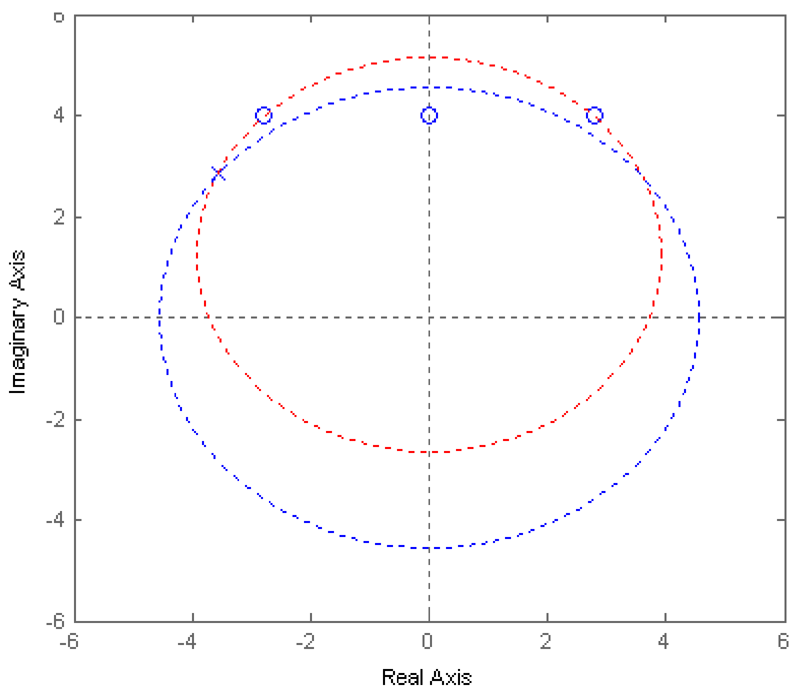

Figure 7 – The cut-off frequency (red dashed line) and dc gain (blue dashed line) conditions that the pole location must meet.

The intersection of these two circles for our example filter is the point -3.57039 + j2.85043.

When three poles are located at this critical point, the frequency response of the analog filter will closely approximate the digital filter's frequency response. A key difference will of course be that the analog filter is valid from 0 rad/s to $\frac{\omega_s}{2}$ rad/s, while the digital filter will operate from 0 rad/s to π rad/s. The frequency response of the calculated *s*-plane zeros and poles is shown overlaid in the figure below with the frequency response of the digital filter.

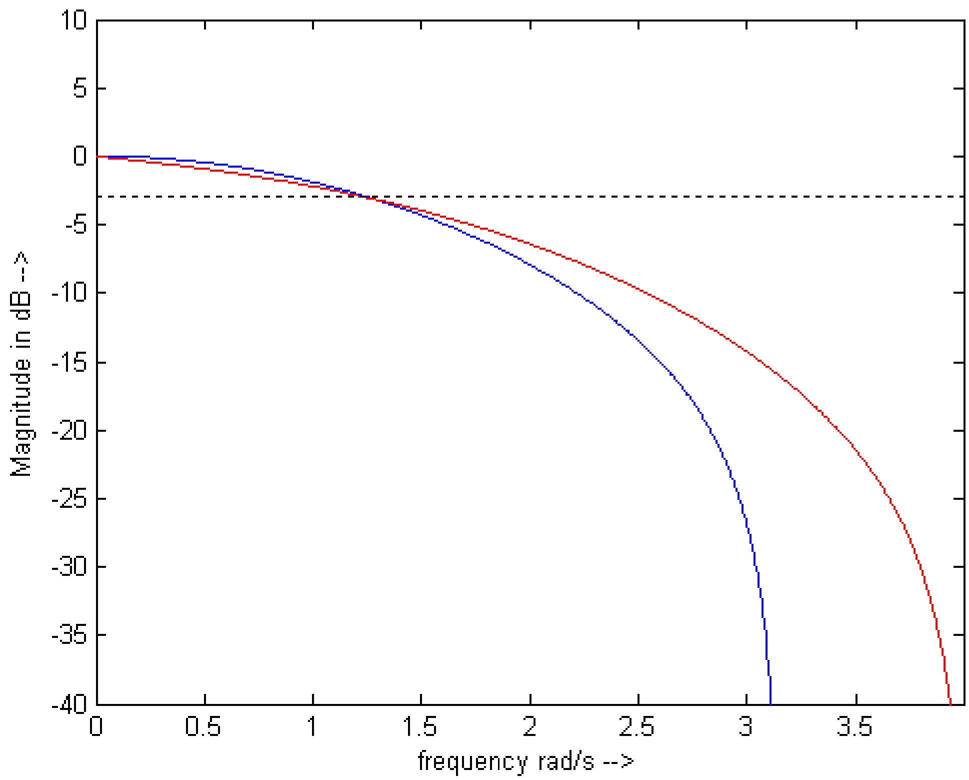

Figure 8 – The frequency response of the analog filter (in red) and the frequency response of the digital filter (in blue). -3.01dB is marked with dashed line.

As Figure 8 shows, the frequency response of the calculated analog filter closely matches that of the digital filter up to approximately 1.5 rad/s, which is beyond the cut-off frequency.

An alternative approach that was tested involved adjusting the poles of the *z*-domain transfer function to be slightly off the origin, such as 0.001 away. However, this resulted in the *s*-plane poles to be located very close to the real axis far into the left-half plane, causing too rapid a drop off in magnitude for the frequency response. The cut-off frequency of this alternative stayed around 0.5 rad/s, well below the specified cut-off frequency of 1.25 rad/s. Determining a new optimal location for the poles using the method described above is possible in the microprocessor and results in a more feasible value to physically implement.

IV. Future Exploration

The work presented in section III is for an FIR filter with a small number of taps and relatively low cutoff and sampling frequencies. This was done to aid in initially exploring the transformation process. Further investigation should be undertaken to judge the validity of the proposed method for higher cutoff and sampling frequencies and FIR filters with a greater number of taps. As the sampling frequency increases, the distribution of zeros and poles on the *s*-plane can become more spread out, and so with a given bank of resistors and capacitors there is conceivably a limit as to the possible cutoff frequencies that can be implemented.

In addition, the latter processes of the proposed method, such as representing the *s*-plane transfer function in standardized active circuit topologies with quantized values, such as those found in [13-14,16], have not yet been addressed.

V. Conclusions

The motivation for this project was to explore a novel way of enabling embedded system designers to take advantage of the benefits offered by true analog signal processing while utilizing existing DSP code and remaining in the digital state of mind. Instead of the quantized time nature of switched-capacitor circuits, this method is truly analog in both time and magnitude.

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