

EE 214 Final Project

2-Stage Telescopic OTA

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Introduction

A fully differential two stage telescopic operational transconductance amplifier for use in a switched capacitor circuit was designed using a gm/Id methodology and simulated in HSPICE using a 0.35 μ m process. This report presents the design process, optimization efforts, and relevant results including frequency response, transient analysis, noise analysis, and corner simulations.

The target specifications for the OTA are shown below in Table 1.

V_{DD}	Load	$A_{V,d}$	Dynamic Range	Settling Time	Static Error	Dynamic Error
3V	≥ 5 pF	1	90 dB	≤ 40 ns	$\leq 0.025\%$	$\leq 0.025\%$

Table 1 – Target Specifications for OTA

The feedback and sample capacitors were to be less than or equal to the load capacitor and be equivalent in value to achieve a unity closed-loop gain. The additional goal was to minimize power. The static error and the dynamic range requirement drove the selection of a suitable topology. The static settling error ϵ_s is found by $\frac{1}{T_o}$, where T_o is the open-loop gain. To achieve less than 0.025% static settling error, an open-loop gain of ≥ 4000 is required. Also a large differential output $V_{od,peak}$ increases the dynamic range for a given noise power. Thus, a two-stage design consisting of a high gain first stage and a large swing common-source second stage was selected. Folded cascode and telescopic configurations were evaluated for the high gain first stage. Both would contribute a gain on the order of $(g_m r_o)^2$, while the second stage would contribute another $g_m r_o$. However, a folded cascode has an additional current branch for its input differential pair, so a telescopic configuration would offer reduced power consumption. The two major weaknesses for a telescopic configuration – poor input common mode range and low output swing are mitigated by the fact that an arbitrary input common mode voltage can be specified for this project and the second stage ensures a large output swing for the overall OTA.

Three variants of this two-stage were designed and simulated: A) PMOS driven telescopic with NMOS driven output stage utilizing Miller compensation, B) NMOS driven telescopic with PMOS driven output stage utilizing Miller compensation, and C) NMOS driven telescopic with PMOS driven output stage utilizing an Ahuja-style cascode compensation technique. Variant A was iterated first, due to the fact that an NMOS driven output stage would have a higher ω_T frequency, thus pole splitting would be achieved more easily. Variant B was iterated on the hypothesis that having NMOS devices in the first stage signal path would result in smaller device dimensions and transconductances, which would help reduce noise. Even after MATLAB-based optimization (as described below), both Variant A and B was estimated to have similar drain currents. Initial results from HSPICE indicated more promise with the NMOS driven telescopic variant, regarding both dynamic range and power consumption. After Variant B was optimized to minimize power, Variant C was tried as an exploration of an Ahuja-style cascode compensation as a way to improve the settling time. Inspiration was found by reading papers from on this technique by Working from the third-order transfer function framework presented in [1] and [2], a design was iterated with very promising current draw estimates calculated in MATLAB, with nearly all the transistors operating near or in the sub-threshold region. However, when the design was ported into HSPICE, the circuit's common-mode feedback showed sustained oscillations and the open-loop gain was only 75% of the expected value. An analysis of the tail and output stage bias currents indicated the slew rate was too low as a result of a very small I_{TAIL} . Attempts to increase common-feedback transconductance and the bias currents to improve the dynamic range and settling-time resulted in this design consuming a similar and/or greater amount of power compared to the Miller compensated NMOS telescopic design. Thus, the final topology chosen was Variant B – an NMOS telescopic first stage with a PMOS driven common-source output stage. While this topology and its associated biasing is simple, for the given specifications it was found to be very suitable both in minimizing power and for stability concerns.

The gain-boosting technique with a single telescopic stage was not considered because though the high open-loop gain needed for the static settling error would have been realizable, it was predicted to be difficult to achieve the 90 dB dynamic range due to the greatly reduced output swing. Additionally, the stability of the gain boosters would also be a major concern for proper performance.

Schematic

Figure 1 shows the telescopic gain stage, the common-source output stage, the CMFB sense and drive components.

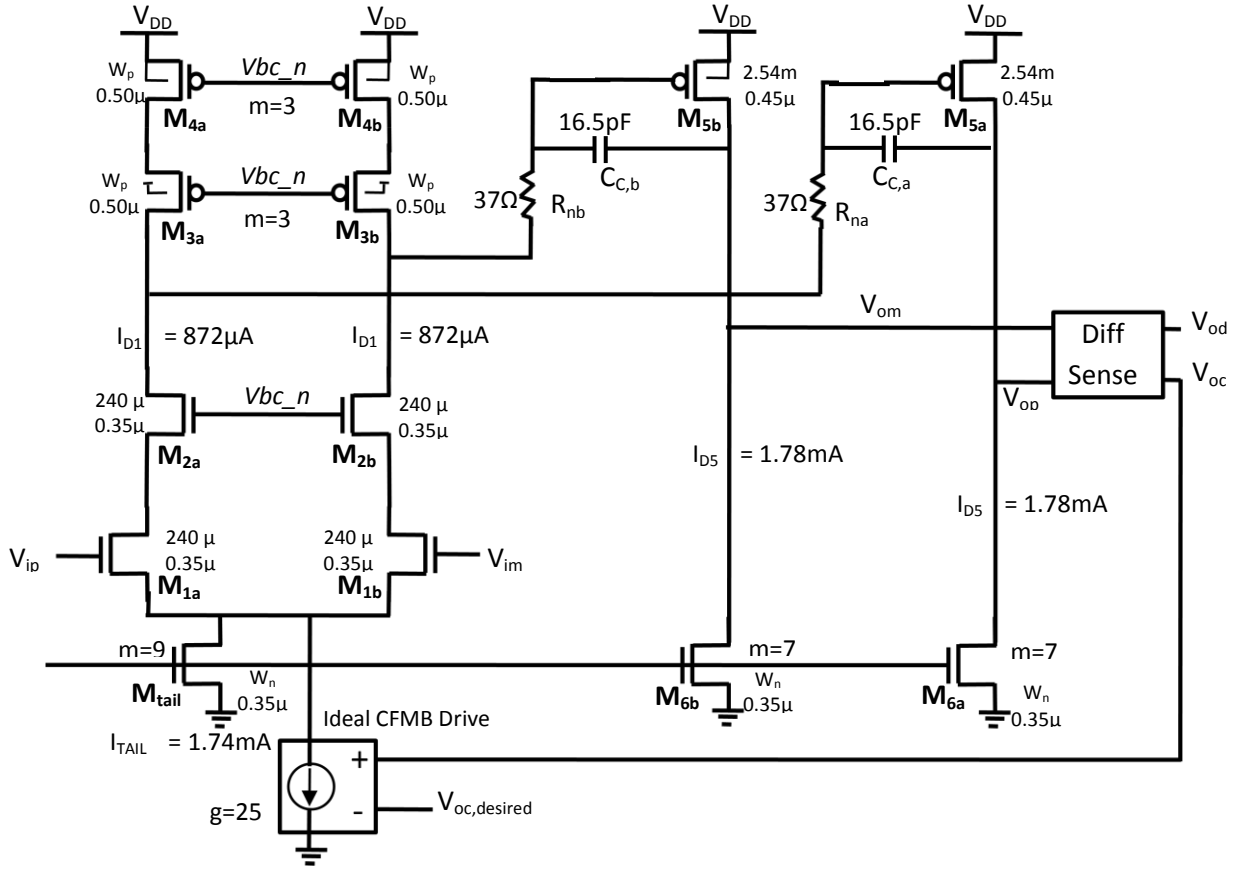
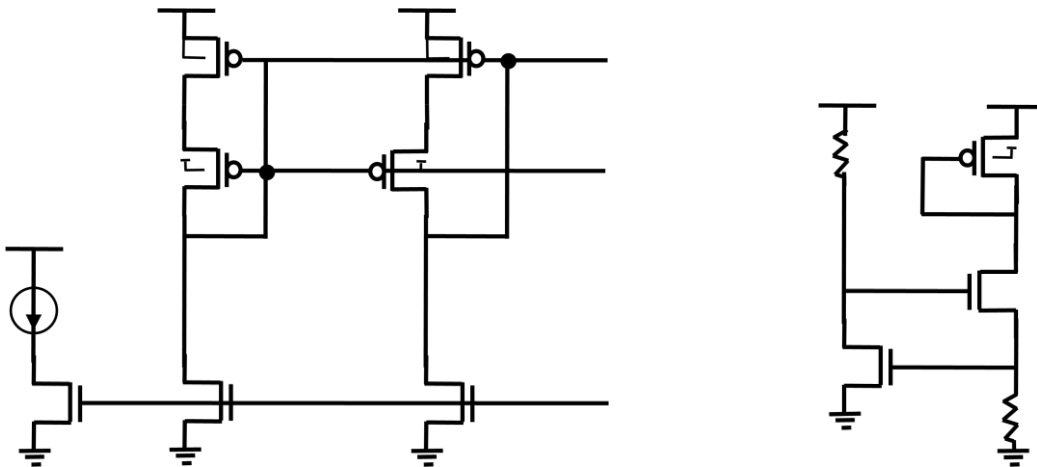


Figure 2 shows the bias network for the OTA.



Page 2: Schematic diagram of final design, with component values and bias currents clearly labeled. Show component values right next to the components, and currents next to the branches (i.e., absolutely, positively do not make us refer to a look-up table). Annotate all transistors with the chosen g_m/I_D value. Clearly indicate the bulk connections for all PMOS devices.

Figure 1 – telescopic & output stage + CMFB

Figure 2 – Bias network

Design Process & Parameter Calculations

A gm/Id design methodology was used as the design process for this OTA. A design flow was created using an example implementation in [3] and consulting [4] for additional insight. Technology characterizations over various parameters were modeled in HSPICE for both NMOS and PMOS then analyzed in MATLAB using an HSPICE toolbox. MATLAB was used as the mathematical engine for the flow because the technology characterization data could be referenced and factored directly in parameter calculations. Technology information was defined, including a minimum length L_{min} of $0.35\mu\text{m}$, an operating temperature of 298K, a γ of $2/3$, and junction capacitance constants of k_{dbn} and k_{dbp} for use in ratiometric design. The load capacitor was chosen to be 5pF, the smallest possible value, for fast operation. The feedback and source capacitors were set to 5pF as well. This design decision was later validated with an extensive MATLAB parameter sweep.

Using a technology characterization plot of gain vs. gm/Id for various device lengths, NMOS lengths of $0.35\mu\text{m}$ and PMOS lengths of $0.50\mu\text{m}$ were chosen because of their matched g_{mro} . An earlier iteration of a PMOS driven telescopic stage revealed that longer lengths create unnecessarily large open-loop gains. The one exception to this is M5a,b, which are the PMOS transistor of the output stage. Its length was set to $0.45\mu\text{m}$ for an increased ω_T .

Next, gm/Id ratios were determined for the signal path and load devices. Each signal path device was set to match its complement load device, and the cascode devices M2a,b and M3a,b were set to match the transistor they were cascoding. Later, reductions in the gm/Id for the cascoded transistors would be tried to lower the noise at the expense of lower swing.

$$g_{41} = \frac{g_{m4}/I_D}{g_{m1}/I_D} := 1 \quad g_{32} = \frac{g_{m3}/I_D}{g_{m2}/I_D} := 1 \quad g_{65} = \frac{g_{m6}/I_D}{g_{m5}/I_D} := 1 \quad g_{21} = \frac{g_{m2}/I_D}{g_{m1}/I_D} := 1 \quad g_{34} = \frac{g_{m3}/I_D}{g_{m4}/I_D} := 1$$

Two iteration parameters are now introduced that will ultimately drive the sizing of transistors in order to satisfy relevant requirements.

$$c_1 = \frac{C_{gg1}}{C_s + C_f} \quad c_2 = \frac{C_{gg2}}{C_L} \quad \text{From the understanding gained in [3], } c_1 \text{ and } c_2 \text{ was set initially to 0.5.}$$

$$C_{gg1} = c_1 * (C_s + C_f) = 0.5 * (5pF + 5pF) := 5pF$$

$$C_{gg2} = c_2 * C_L = 0.5 * 5pF := 2.5pF$$

Note that the estimate for the feedback factor β also changes.

$$\beta = \frac{C_f}{(C_f + C_s)(c_1(C_f + C_s))} = \frac{C_f}{(C_f + C_s)(1 + c_1)} = 0.33$$

To estimate junction capacitances such as C_{db} , the ratiometric approach using k_{dbn} and k_{dbp} was used. A small signal analysis showed that the C_{gd2} and C_{gd3} are present at the output of the telescopic stage and C_{gd5} and C_{gd6} are present at the output of the second stage, but for the purposes of the initial design they were assumed to be not as significant as the C_{db} capacitance based on the technology characterization plot for C_{db}/C_{gg} and C_{gd}/C_{gg} . This would be later verified in simulation.

$$C_{db1} = k_{dbn} \times C_{gg1} \times \frac{L_{min}}{L_1} = 3.25pF$$

Because the junction capacitances depend on the device dimension, a ratiometric and gm/Id based approach is needed to relate the device widths. Using an initial estimate of gm/Id, values from the technology characterization data were interpolated. To keep overdrive voltages low, a value of $gm/Id_1 = gm/Id_5 = 14$ was chosen.

$$w_{41} = \frac{nidw(L_1, 14S/A)}{pidw(L_4, 14S/A \times g_{41})} = 5.91 \quad C_{db4} = w_{41} \times C_{db1} \times \frac{k_{dbp}}{k_{dbn}} = 23.6pF$$

$$C_{db2} = g_{21} \times C_{db1} = 3.25pF \quad C_{db3} = g_{34} \times C_{db4} = 23.6pF \quad C_{db5} = k_{dbp} \times C_{gg2} \times \frac{L_{min}}{L_5} = 1.56pF$$

$$w_{65} = \frac{pidw(L_1, 14S/A)}{nidw(L_4, 14S/A \times g_{65})} = 0.23 \quad C_{db6} = w_{65} \times C_{db5} \times \frac{k_{dbn}}{k_{dbp}} = 295fF$$

With approximations for the junction capacitances, the stage 1 and stage 2 loads could be estimated.

$$C_{stage1} = C_{db2} + C_{db3} + C_{gg2} = 29.4 pF \quad C_{stage2} = C_{db5} + C_{db6} + C_L + (1 - \beta)C_f = 10.2 pF$$

The final significant capacitor that must be calculated is the Miller compensation capacitor. This Miller compensation serves to create a dominant pole by increasing the effective capacitance the telescopic stage sees and decreasing the capacitance the output node sees. The result is that a desired phase margin can be more easily achieved at the unity-gain frequency of the open-loop transfer function, which corresponds to the f_{-3dB} frequency of the closed-loop transfer function. The value of the compensation capacitor is primarily driven by the dynamic range requirement, as this capacitor reduces the noise from the telescopic stage. The iteration script ignores the noise contribution from the cascode stage. This was a result of insight from [3] and [4]. While flicker noise would be present, its effect on total integrated noise was predicted to be small. To determine the needed noise power to satisfy the dynamic range calculation, the differential output peak voltage was estimated and a conservative dynamic range value of 91 dB was used. The estimated overdrive voltages for M5 and M6 were 160mV. This was informed by previous simulations for Variant A. This differs slightly from long-channel equations.

$$V_{od,peak} = V_{DD} - |V_{Dsat5}| - V_{Dsat6} = 3 - 0.16 - 0.16 = 2.68V \quad N_{tot} = \frac{1/2 V_{od,peak}^2}{10^{\frac{DR_{dB}}{20}}} = 2.85 nV^2$$

Now the noise power is expressed in terms of circuit parameters, ignoring flicker noise.

$$N_{tot} = 2 \times \frac{k_B T}{\beta \times C_c} \gamma (1 + g_{41}) + \frac{k_B T}{C_{stage2}} \gamma (1 + g_{65}) + 1 \times \frac{k_B T}{C_c} \gamma (1 + g_{65})$$

which leads to a $C_c = 34.3 pF$.

Next, the dynamic settling error and settling time was used to determine a suitable closed loop frequency. The following expression refers to the linear settling time, and this was chosen as 20 ns to allow a time margin for slewing. The intent was to over-design the OTA in MATLAB to help account for assumptions and possible second order effects. The dynamic settling error was set as 0.023%. A phase margin (PM) of 75° was desired for optimal transient response. A scaling factor k was introduced in order to determine how far to shift the non-dominant pole f_{p2} higher than f_c .

$$f_c = -\frac{1}{2\pi \times \tau_s} \ln(\epsilon_d) := -\frac{1}{2\pi \times 20e-9} \log(0.00023) := 66.67 MHz \quad k = \tan\left(\frac{PM}{180}\right) \times \frac{PM}{180} = 3.73$$

The transconductances and transit frequencies of M1 and M5 could thus be calculated.

$$g_{m1} = \frac{1}{\beta} \times 2\pi \times f_c \times C_c = 43.1 mS \quad g_{m2} = k \times 2\pi \times f_c \times \frac{C_{stage1} \times C_{stage2}}{C_c} + C_{stage1} + C_{stage2} = 75.5 mS$$

$$f_{T1} = \frac{g_{m1}}{2\pi \times C_{gg1}} = 1.37 GHz \quad f_{T5} = \frac{g_{m5}}{2\pi \times C_{gg2}} = 4.81 GHz$$

The technology characterization data was used to determine the actual gm/Id values for the specified f_t , L.

$$g_m / I_{D1} = 21.53 S/A \quad g_m / I_{D5} = 3.96 S/A \quad I_{D1} = \frac{g_{m1}}{g_m / I_{D1}} = 2 mA \quad I_{D5} = \frac{g_{m5}}{g_m / I_{D5}} = 19.1 mA$$

Thus, the total current without biasing is $I_{Tot} = 2 \times I_{D1} + 2 \times I_{D5} = I_{TAIL} + 2 \times I_{D5} = 42.2 mA$

In MATLAB, the design parameters c_1 and c_2 were each iterated from 0.01 to 0.95 in 0.005 steps, and the total current was recorded for each (c_1, c_2) . Additionally, this process was repeated for each C_L from 5pF to 15pF in 0.5pF steps and the corresponding C_s and C_f of 1pF to C_L in 0.5pF steps. This four parameter iteration was then analyzed to find the combination of C_L , C_s and C_f , c_1 , and c_2 that would result in the lowest total current. For brevity, the re-calculated values of all the above circuit parameters will not be shown for these four optimized values. Relevant parameters to the operation and requirements of the OTA are shown in Table 2.

$$C_{L,opt} = 5 pF \quad C_{f,opt} = C_{s,opt} = 5 pF \quad c_{1,opt} = 0.04 \quad c_{2,opt} = 0.89$$

A nulling resistor R_n in series with C_c creates a zero in the amplifier transfer function. As shown in [3], setting R_n to slightly less than $1/g_{m5}$ pushes the zero to near positive infinity, which helps to mitigate its effect on the phase. In practice, this resistor would be implemented with a triode transistor to ensure tracking over process variations. The nulling resistor will contribute thermal noise to the output of the amplifier, but this is assumed to be not as significant as the noise sources described above. This assumption will be validated in simulation. The new total current = 7.71mA. Assuming the biasing is

30% of that, the estimated power is 30.1 mW. The settling time was calculated by combining slewing time and linear settling time, using an input step of 2.45V.

$$t_s = \frac{|V_{step}| - \frac{2.8}{\beta \times SR} (g_m/I_{D1})}{2\pi \times f_c} \ln(\epsilon_d), \text{ with } SR = \frac{I_{TAIL}}{C_{Ltot}} = 3.77e8 \text{ @ } t_s = 12.4nS + 20nS = 32.4nS$$

A wide-swing cascode current mirror was implemented to bias the PMOS cascode current source load of the telescopic stage. As described in [3], the triode transistor Mb2a was set with at $1/5^{\text{th}}$. A V_t referenced bias circuit was used to bias the NMOS cascode M3. This avoided slowing down any existing nodes in the existing circuit, either in the bias network or the two stages. Mtail and M6 were biased from the same NMOS bias reference, which accepted the ideal current source I_{REF} . Though the width and current ratios between Mtail and M6 differ, the difference was determined to be not too significant. The input common mode voltage was set to keep Mtail at the edge of triode, to ensure a small V_{OV} . The NMOS bias voltage was set in a similar fashion, except to keep M1 at the edge of triode. Initial simulations revealed the V_{DS} differences in the cascode current source were causing significant current mirror deviations, so I_{REF} was reduced until the desired bias currents were achieved. An input differential step of 2.45V satisfied the dynamic range. A set of MATLAB scripts utilizing the HSPICE toolbox were used to calculate parameters such as DR, N_{Tot} , t_s , and ϵ_s .

Parameter	MATLAB Optimized	First Pass Simulation	Final Optimized Simulation
β	0.48	0.48	0.48
C_{stage1}, C_{stage2}	6.6pF, 10.9pF	7.97pF, 12.1pF	5.8pF, 12.1pF
Output Swing	2.65V	2.75V	2.78V
N_{tot}, V_{rms}	53.4 μV_{rms}	51.98 μV_{rms}	53.85 μV_{rms}
C_c, R_n	21pF, 30.6 Ω	21pF, 30.6 Ω	16.5pF, 37 Ω
g_{m1}, g_{m5}	18.4mS, 32.7mS	18.3mS, 33.4mS	12.89mS, 25.8mS
I_{D1}, I_{D5}	1.43mA, 2.42mA	1.44mA, 2.51mA	0.872mA, 1.78mA
$g_m/I_{D1}, g_m/I_{D5}$	12.8 S/A, 13.4 S/A	12.7 S/A, 13.3 S/A	14.8 S/A, 13.5 S/A
f_c, PM	66.6MHz, 75 $^\circ$	55.5MHz, 78.1 $^\circ$	53.40 MHz, 76.8$^\circ$
Power	30.1mW (est)	27.2mW	18.67mW
DR	91 dB	90.28 dB	90.15 dB
t_s	32.4 nS	33.3ns	33.48 nS
$ \epsilon_s $	0.023%	0.017%	0.019%

Table 2- MATLAB Calculated Values vs Simulation Values from the .op listing

To first order, the first pass simulation matches quite well to the MATLAB calculated values. As expected, the C_{stage} loads are 20% higher in SPICE due to the additional parasitic junction capacitances at the drains, and thus f_c is lower. The g_m/I_D values match, as does the settling time. The lower ϵ_s indicates additional open-loop gain, which is an acceptable improvement. Additionally, the 30% current approximation for biasing was slightly conservative, as the first pass simulation shows a power draw of 27.2mW. A word should be said concerning the ideal common-mode feedback (CMFB) sense and drive circuit. The desired output common-mode was 1.5V, to allow for maximum swing between the rails. To ensure fast settling and stability of the common-mode output, the transconductance of the 'g' element was chosen to be comparable to the transconductance of M1, thus emulating the differential signal path. A transient analysis of the common-mode output shows that the CM is stable. An extended discussion of CMFB for all three circuit versions shown in Table 2, can be found in the commentary for the common-mode voltage transient plot.

To further optimize the circuit and to minimize power, I_{REF} and the m-factors for M3, M4, Mtail, and M6 were iterated to lower values. The motivation was to maintain similar I_{D1}/I_{D5} ratios as previously calculated, but use less current. Ultimately, g_m/I_{D1} was increased by 17% while g_m/I_{D5} stayed the same. This change lowered the V_{ov} of the input pair. As the current was lowered, the values of the nulling resistor and C_c were changed to fine tune to the step response. It was observed that a smaller C_c caused the transient to rise faster with a greater overshoot, but slightly increasing R_n allowed the waveform to still settle within the static error bounds. Great care was taken to ensure that $R_n < 1/g_{m5}$, thus avoiding LHP zeros. At the smaller C_c , the dynamic range decreased by ~ 0.5 dB due to greater noise power at the output. It can be argued that the design assumption to ignore the noise contribution from the cascode transistors and the nulling resistor was acceptable, seeing as the simulated $N_{tot, Vrms}$ varied between 1% and 2.6% of the calculated value. The output noise for

the final optimized circuit remains at the same level as before despite a decrease in I_D and g_m due to the lower C_c and higher R_n , but still the dynamic range specification remained within bound.

Frequency Response: Bode Plot of $T(\omega)$

Page 6: Bode plot of $T(j\omega)$, phase and magnitude. Clearly annotate the achieved low frequency loop gain, the loop crossover frequency and the phase margin.

Figure 3 – $T(j\omega)$ magnitude

Figure 4 – $T(j\omega)$ phase

Transient Analysis

Page 7: Plot the simulated settling transient of V_{od} (no zoom, show the entire waveform). In a separate subplot, show the % error of the differential output voltage relative to the ideal output voltage. Zoom into the relevant region of the settling, i.e. clearly demonstrate that your design settles within spec. Annotate the achieved settling time and static settling error. For simplicity, we use the error at $t = \text{twice the settling time spec}$ as an estimate of the static settling error.

Figure 5 – Settling transient of V_{od} , full scale

Figure 6 - % error of differential $V_{od}/(\text{ideal output voltage})$

Figure 7 – Zoom into relevant region of settling

Common Mode Voltage Analysis

Page 8: Plot the common mode output voltage versus time during transient settling of the circuit. In separate subplots each, also show the differential output current of the OTA, and the differential input to the OTA (V_{id} in Figure 1).

Figure 8 – Common mode output voltage vs time

Figure 9 – differential output current of OTA

Figure 10 – differential input to the OTA

Noise Analysis

Page 9: Plot of the noise power spectral density at the OTA output (V_{od}) and noise integral. Annotate the total integrated noise value and the achieved dynamic range.

Figure 11 – Noise power spectral density at the OTA output V_{od}

Figure 12 – Noise integral

Output Range

Page 10: Output range. Simulation plot showing the differential open loop DC gain V_{od}/V_{id} of the amplifier. Mark the differential output voltage at which the gain has dropped by 30%. This value should be larger than the peak output voltage used in your dynamic range calculation.

Figure 13 – Plot output range, open loop DC gain V_{od}/V_{id} of the amplifier. UNNORMALIZED.

Corner Simulations

Page 11-12: Results of corner simulations. Tabulate your circuit's performance for the slow/hot and fast/cold corner. Include settling time, static error, and any other parameter that you find noteworthy. Include the %-changes with respect to nominal conditions in your table. In case the circuit is non-functional in these corners, investigate and explain the problem (no need to fix the circuit). Include selected interesting plots documenting corner performance and/or issues.

Figure 14 – Plot showing frequency response for nominal/fast/slow

Figure 15 – Plot showing transient response for nominal/fast/slow

Conclusion

References & Appendices

- [1] Libin Yao; Steyaert, M.; Sansen, W.; "Fast-Settling CMOS Two Stage Operational Transconductance Amplifiers and Their Systematic Design." IEEE Int'l Symposium on Circuits and Systems, 2002: ISCAS 2002. Volume 2, 26-29 May 2002. Pages(s) II-839-II-842.
- [2] Kashmiri, S.M.; Hedayati, H.; Shoaie, O.; "Systematic steps in design of a CMOS two-stage cascode-compensated OTA." Proceedings of the 15th Int'l Conference on Microelectronics. ICM 2003. 9-11 Dec. 2003. Page(s) 409-412.
- [3] Murmann, Boris. "EE 214 Course Reader: Analog Integrated Circuit Design." Fall 2007. Page(s) 246-257.
- [4] Cortes, Fernando Paixão and Sergio Bampi. "Miller OTA Design using a Design Methodology Based on the gm/Id and Early-Voltage Characteristics: Design Considerations and Experimental Results." Federal University of Rio Grande do Sul (UFRGS). Informatics Institute.

In a switched capacitor circuit, the feedback and sampling capacitors serve as a capacitive divider along with the input capacitance to the OTA. This is factored into the loop gain expression as a feedback factor, β .

$$\beta = \frac{C_f}{C_f + C_s + C_{gg1}}$$
 Initially, the input capacitance C_{gg1} was assumed to equal the sum of C_s and C_f . This resulted in a $\beta = 0.25$.

Loop gain required $1/(e s \cdot \beta)$ Explain how each transistor contributes gmro, so the open loop cube-rooted, and so on