

EE 214 Final Project

Fully Differential 2-Stage Telescopic OTA

Saket Vora & Nader Moussa
December 6, 2007

Dr. Boris Murmann
Stanford University

Introduction

A fully differential two stage telescopic operational transconductance amplifier for use in a switched capacitor circuit was designed using a gm/Id methodology and simulated in HSPICE using a 0.35 μ m process. This report presents the design process, optimization efforts, and relevant results including frequency response, transient analysis, noise analysis, and corner simulations.

The target specifications for the OTA are shown below in Table 1.

| V_{DD} | Load | $A_{V,cl}$ | Dynamic Range | Settling Time | Static Error | Dynamic Error |
|----------|------------|------------|---------------|---------------|----------------|----------------|
| 3V | $\geq 5pF$ | 1 | 90 dB | $\leq 40ns$ | $\leq 0.025\%$ | $\leq 0.025\%$ |

Table 1 – Target Specifications for OTA

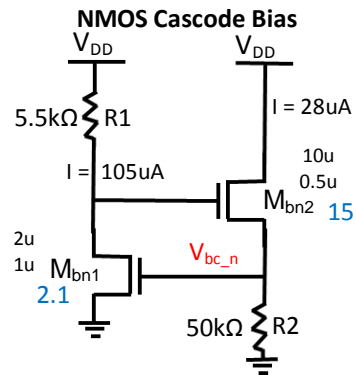
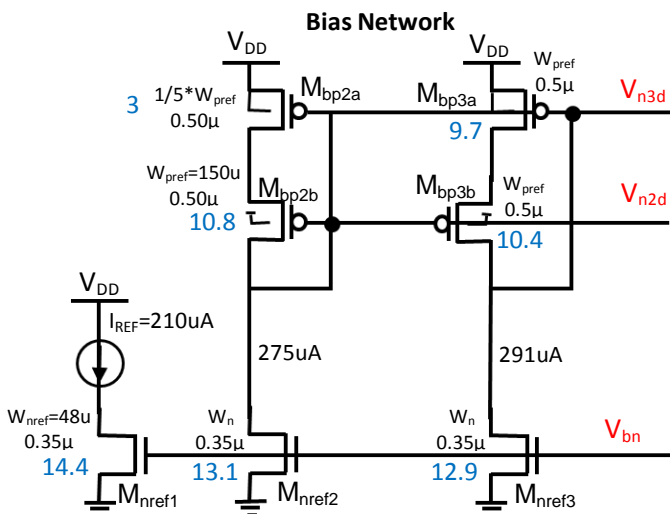
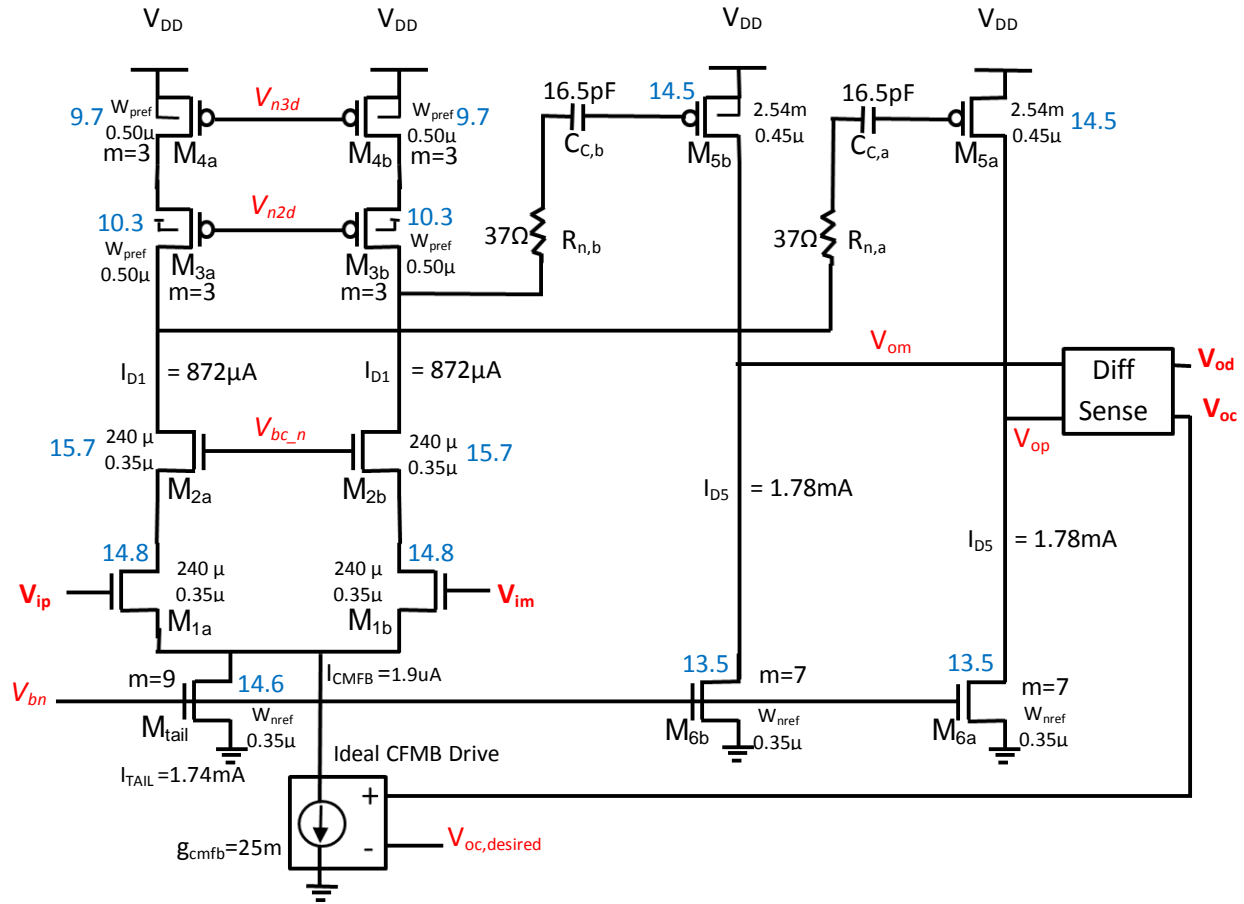
The feedback and sample capacitors were to be less than or equal to the load capacitor and be equivalent in value to achieve a unity closed-loop gain. The additional goal was to minimize power. The static error and the dynamic range requirement drove the selection of a suitable topology. The static settling error ϵ_s is found by $\frac{1}{T_0}$, where T_0 is the open-loop gain. To achieve less than 0.025% static settling error, an open-loop gain of ≥ 4000 is required. Also a large differential output $V_{od,peak}$ increases the dynamic range for a given noise power. Thus, a two-stage design consisting of a high gain first stage and a large swing common-source second stage was selected. Folded cascode and telescopic configurations were evaluated for the high gain first stage. Both would contribute a gain on the order of $(g_m r_o)^2$, while the second stage would contribute another $g_m r_o$. However, a folded cascode has an additional current branch for its input differential pair, so a telescopic configuration would offer reduced power consumption. The two major weaknesses for a telescopic configuration – poor input common mode range and low output swing are mitigated by the fact that an arbitrary input common mode voltage can be specified for this project and the second stage ensures a large output swing for the overall OTA.

Three variants of this two-stage were designed and simulated: A) PMOS driven telescopic with NMOS driven output stage utilizing Miller compensation, B) NMOS driven telescopic with PMOS driven output stage utilizing Miller compensation, and C) NMOS driven telescopic with PMOS driven output stage utilizing an Ahuja-style cascode compensation technique. Variant A was iterated first, due to the fact that an NMOS driven output stage would have a higher ω_T frequency, thus pole splitting would be achieved more easily. Variant B was iterated on the hypothesis that having NMOS devices in the first stage signal path would result in smaller device dimensions and transconductances, which would help reduce noise. Even after MATLAB-based optimization (as described below), both Variant A and B was estimated to have similar drain currents. Initial results from HSPICE indicated more promise with the NMOS driven telescopic variant, regarding both dynamic range and power consumption. After Variant B was optimized to minimize power, Variant C was tried as an exploration of an Ahuja-style cascode compensation as a way to improve the settling time. Inspiration was found by reading papers from on this technique by Working from the third-order transfer function framework presented in [1] and [2], a design was iterated with very promising current draw estimates calculated in MATLAB, with nearly all the transistors operating near or in the sub-threshold region. However, when the design was ported into HSPICE, the circuit's common-mode feedback showed sustained oscillations and the open-loop gain was only 75% of the expected value. An analysis of the tail and output stage bias currents indicated the slew rate was too low as a result of a very small I_{TAIL} . Attempts to increase common-feedback transconductance and the bias currents to improve the dynamic range and settling-time resulted in this design consuming a similar and/or greater amount of power compared to the Miller compensated NMOS telescopic design. Thus, the final topology chosen was Variant B – an NMOS telescopic first stage with a PMOS driven common-source output stage. While this topology and its associated biasing is simple, for the given specifications it was found to be very suitable both in minimizing power and for stability concerns.

The gain-boosting technique with a single telescopic stage was not considered because though the high open-loop gain needed for the static settling error would have been realizable, it was predicted to be difficult to achieve the 90 dB dynamic range due to the greatly reduced output swing. Additionally, the stability of the gain boosters would also be a major concern for proper performance.

Schematic

Figure 1 shows the telescopic gain stage, the common-source output stage, the CMFB sense and drive components.



All PMOS bulks are connected to V_{DD}
 All NMOS bulks are connected to ground.

| Legend | |
|------------|-------------|
| V_{node} | in red |
| g_m/I_D | in blue |
| \square | bulk to vdd |

Figure 1 - Schematic

Design Process & Parameter Calculations

A gm/Id design methodology was used as the design process for this OTA. A design flow was created using an example implementation in [3] and consulting [4] for additional insight. Technology characterizations over various parameters were modeled in HSPICE for both NMOS and PMOS then analyzed in MATLAB using an HSPICE toolbox. MATLAB was used as the mathematical engine for the flow because the technology characterization data could be referenced and factored directly in parameter calculations. Technology information was defined, including a minimum length L_{min} of $0.35\mu\text{m}$, an operating temperature of 298K , a γ of $2/3$, and junction capacitance constants of k_{dbn} and k_{dbp} for use in ratiometric design. The load capacitor was chosen to be 5pF , the smallest possible value, for fast operation. The feedback and source capacitors were set to 5pF as well. This design decision was later validated with an extensive MATLAB parameter sweep.

Using a technology characterization plot of gain vs. gm/Id for various device lengths, NMOS lengths of $0.35\mu\text{m}$ and PMOS lengths of $0.50\mu\text{m}$ were chosen because of their matched g_{mro} . An earlier iteration of a PMOS driven telescopic stage revealed that longer lengths create unnecessarily large open-loop gains. The one exception to this is M5a,b, which are the PMOS transistor of the output stage. Its length was set to $0.45\mu\text{m}$ for an increased ω_T .

Next, gm/Id ratios were determined for the signal path and load devices. Each signal path device was set to match its complement load device, and the cascode devices M2a,b and M3a,b were set to match the transistor they were cascoding. Later, reductions in the gm/Id for the cascoded transistors would be tried to lower the noise at the expense of lower swing.

$$g_{41} = \frac{g_{m4}/I_D}{g_{m1}/I_D} := 1 \quad g_{32} = \frac{g_{m3}/I_D}{g_{m2}/I_D} := 1 \quad g_{65} = \frac{g_{m6}/I_D}{g_{m5}/I_D} := 1 \quad g_{21} = \frac{g_{m2}/I_D}{g_{m1}/I_D} := 1 \quad g_{34} = \frac{g_{m3}/I_D}{g_{m4}/I_D} := 1$$

Two iteration parameters are now introduced that will ultimately drive the sizing of transistors in order to satisfy relevant requirements.

$$c_1 = \frac{C_{gg1}}{C_s + C_f} \quad c_2 = \frac{C_{gg2}}{C_L} \quad \text{From the understanding gained in [3], } c_1 \text{ and } c_2 \text{ was set initially to } 0.5.$$

$$C_{gg1} = c_1 * (C_s + C_f) = 0.5 * (5\text{pF} + 5\text{pF}) := 5\text{pF} \quad C_{gg2} = c_2 * C_L = 0.5 * 5\text{pF} := 2.5\text{pF}$$

Note that the estimate for the feedback factor β also changes.

$$\beta = \frac{C_f}{(C_f + C_s)(c_1 \cdot (C_f + C_s))} = \frac{C_f}{(C_f + C_s)(1 + c_1)} = 0.33$$

To estimate junction capacitances such as C_{db} , the ratiometric approach using k_{dbn} and k_{dbp} was used. A small signal analysis showed that the C_{gd2} and C_{gd3} are present at the first stage output and C_{gd5} and C_{gd6} are present at the second stage output, but for the purposes of the initial design they were assumed to be not as significant as the C_{db} capacitance based on the technology characterization plot for C_{db}/C_{gg} and C_{gd}/C_{gg} . This would be later verified in simulation. Because the junction capacitances depend on the device dimension, a ratiometric and gm/Id based approach is needed to relate the device widths. Using an initial estimate of gm/Id, values from the technology characterization data were interpolated. To keep overdrive voltages low, a value of $gm/Id_1 = gm/Id_5 = 14$ was chosen.

$$C_{db1} = k_{dbn} \cdot C_{gg1} \cdot \frac{L_{min}}{L_1} = 3.25\text{pF} \quad w_{41} = \frac{nidw(L_1, 14\text{S}/A)}{pidw(L_4, 14\text{S}/A \cdot g_{41})} = 5.91 \quad ; \quad C_{db4} = w_{41} \cdot C_{db1} \cdot \frac{k_{dbp}}{k_{dbn}} = 23.6\text{pF}$$

$$C_{db2} = g_{21} \cdot C_{db1} = 3.25\text{pF} \quad C_{db3} = g_{34} \cdot C_{db4} = 23.6\text{pF} \quad C_{db5} = k_{dbp} \cdot C_{gg2} \cdot \frac{L_{min}}{L_5} = 1.56\text{pF}$$

$$w_{65} = \frac{pidw(L_1, 14\text{S}/A)}{nidw(L_4, 14\text{S}/A \cdot g_{65})} = 0.23 \quad C_{db6} = w_{65} \cdot C_{db5} \cdot \frac{k_{dbn}}{k_{dbp}} = 295\text{fF}$$

With approximations for the junction capacitances, the stage 1 and stage 2 loads could be estimated.

$$C_{stage1} = C_{db2} + C_{db3} + C_{gg2} = 29.4\text{pF} \quad C_{stage2} = C_{db5} + C_{db6} + C_L + (1 - \beta)C_f = 10.2\text{pF}$$

The final significant capacitor that must be calculated is the Miller compensation capacitor. This Miller compensation serves to create a dominant pole by increasing the effective capacitance the telescopic stage sees and decreasing the

capacitance the output node sees. The result is that a desired phase margin can be more easily achieved at the unity-gain frequency of the open-loop transfer function, which corresponds to the f_{-3dB} frequency of the closed-loop transfer function. The value of the compensation capacitor is primarily driven by the dynamic range requirement, as this capacitor reduces the noise from the telescopic stage. The iteration script ignores the noise contribution from the cascode stage. This was a result of insight from [3] and [4]. While flicker noise would be present, its effect on total integrated noise was predicted to be small. To determine the noise power needed to satisfy the dynamic range, the differential output peak voltage was estimated and a conservative dynamic range of 91 dB was used. The estimated overdrive voltages for M5 and M6 were 160mV. This was informed by previous simulations for Variant A, differing from long-channel equations.

$$V_{od,peak} = V_{DD} - |V_{Dsat5}| - V_{Dsat6} = 3 - 0.16 - 0.16 = 2.68V \quad N_{tot} = \frac{1/2 V_{od,peak}^2}{10^{(DR/10)}} = 2.85nV^2 \rightarrow 53.39 \mu V_{rms}$$

Now the noise power is expressed in terms of circuit parameters, ignoring flicker noise.

$$N_{tot} = 2 \cdot \left[\frac{k_B T}{\beta \cdot C_c} \gamma (1 + g_{41}) + \frac{k_B T}{C_{stage2}} [\gamma (1 + g_{65})] + 1 \right], \text{ which leads to a } C_c = 34.3pF.$$

Next, the dynamic settling error and settling time spec was used to determine a suitable closed loop frequency. The following expression refers to the linear settling time, and this was chosen as 20 ns to allow a time margin for slewing. The intent was to over-design the OTA in MATLAB to help account for assumptions and possible second order effects. The dynamic settling error was set as 0.023%. A phase margin (PM) of 75° was desired for optimal transient response. A scaling factor k was introduced in order to determine how far to shift the non-dominant pole f_{p2} higher than f_c .

$$f_c = -\frac{1}{2\pi \cdot t_s} \ln(\epsilon_d) := -\frac{1}{2\pi \cdot 20e-9} \log(0.00023) := 66.67 \text{ MHz} \quad k = \tan\left(\pi \cdot \frac{PM}{180^\circ}\right) = 3.73$$

The transconductances and transit frequencies of M1 and M5 could thus be calculated.

$$g_{m1} = \frac{1}{\beta} \cdot 2\pi \cdot f_c \cdot C_c = 43.1mS \quad g_{m2} = k \cdot 2\pi \cdot f_c \cdot \left(\frac{C_{stage1} \cdot C_{stage2}}{C_c} + C_{stage1} + C_{stage2} \right) = 75.5mS$$

These large g_m values were a major sign of an unoptimized design. They will be difficult to achieve without a large width.

$$f_{T1} = \frac{g_{m1}}{2\pi \cdot C_{gg1}} = 1.37GHz \quad f_{T5} = \frac{g_{m5}}{2\pi \cdot C_{gg2}} = 4.81GHz$$

The technology characterization data was used to determine the actual gm/Id values for the specified f_t , L.

$$g_m/I_{D1} = 21.53 \text{ S/A} \quad g_m/I_{D5} = 3.96 \text{ S/A} \quad I_{D1} = \frac{g_{m1}}{g_m/I_{D1}} = 2mA \quad I_{D5} = \frac{g_{m5}}{g_m/I_{D5}} = 19.1mA$$

$$\text{Thus, the total current without biasing is } I_{Tot} = 2 \cdot I_{D1} + 2 \cdot I_{D5} = I_{TAIL} + 2 \cdot I_{D5} = 42.2mA$$

This current is very asymmetric, a sign that the output stage is having to very hard. A balanced distribution of currents were desired. In MATLAB, the design parameters c_1 and c_2 were each iterated from 0.01 to 0.95 in 0.005 steps, and the total current was recorded for each (c_1, c_2) . Additionally, this process was repeated for each C_L from 5pF to 15pF in 0.5pF steps and the corresponding C_s and C_f of 1pF to C_L in 0.5pF steps. This four parameter iteration was then analyzed to find the combination of C_L , C_s and C_f , c_1 , and c_2 that would result in the lowest total current. For brevity, the re-calculated values of *all* the above circuit parameters will not be shown for these four optimized values. Relevant parameters to the operation and requirements of the OTA are shown in Table 2 and discussed below.

$$C_{L,opt} = 5pF \quad C_{f,opt} = C_{s,opt} = 5pF \quad c_{1,opt} = 0.04 \quad c_{2,opt} = 0.89$$

The minimum C_L aids in increasing the slew rate, which improves settling time. A nulling resistor R_n in series with C_c creates a zero in the amplifier transfer function. As shown in [3], setting R_n to slightly less than $1/g_{m5}$ pushes the zero to near positive infinity, which helps to mitigate its effect on the phase. In practice, this resistor would be implemented with a triode transistor to ensure tracking over process variations. The new total current = 7.71mA. Assuming the biasing is 30% of that, the estimated power is 30.1 mW. The settling time was calculated by combining slewing time and linear settling time, shown respectively in the equation below, using an input step of 2.45V.

$$t_s = \frac{|V_{step}|^{-2.8} / (g_m / I_{D1})}{\beta \cdot SR} - \frac{1}{2\pi \cdot f_c} \ln(\epsilon_d), \text{ with } SR = \frac{I_{TAIL}}{C_{Ltot}} = 3.77e8 \rightarrow t_s = 12.4nS + 20nS = 32.4nS$$

A wide-swing cascode current mirror was implemented to bias the PMOS cascode current source load of the telescopic stage. As described in [3], the triode transistor Mb2a was set with at $1/5^{\text{th}}$. A V_t referenced bias circuit was used to bias the NMOS cascode M3. This avoided slowing down any existing nodes in the existing circuit, either in the bias network or in the two stages. Mtail and M6 were biased from the same NMOS bias reference, which accepted the ideal current source I_{REF} . Though the width and current ratios between Mtail and M6 differ, the difference was determined to be not too significant. The input common mode voltage was set to keep Mtail at the edge of triode, to ensure a small V_{OV} . The NMOS bias voltage was set in a similar fashion, except to keep M1 at the edge of triode. Initial simulations revealed the V_{DS} differences in the cascode current source were causing elevated mirror currents, so I_{REF} was reduced until the desired bias currents were achieved in the gain stages. An input differential step of 2.45V satisfied the dynamic range. A set of MATLAB scripts utilizing the HSPICE toolbox were used to calculate specification parameters such as DR, N_{Tot} , t_s , and ϵ_s .

| Parameter | MATLAB First Pass* | MATLAB Optimized | First Pass Simulation | Final Optimized Simulation |
|--------------------------|-----------------------|----------------------|------------------------|---|
| β | 0.33 | 0.48 | 0.48 | 0.48 |
| C_{stage1}, C_{stage2} | 29.4pF, 10.2pF | 6.6pF, 10.9pF | 7.97pF, 12.1pF | 5.8pF, 12.1pF |
| Output Swing | 2.65V | 2.65V | 2.75V | 2.78V |
| N_{tot}, V_{rms} | 53.4 μV_{rms} | 53.4 μV_{rms} | 51.98 μV_{rms} | 52.46 μV_{rms} |
| C_c, R_n | 34.4pF, 13.2 Ω | 21pF, 30.6 Ω | 21pF, 30.6 Ω | 16.5pF, 37 Ω |
| g_{m1}, g_{m5} | 43.1mS, 75.5mS | 18.4mS, 32.7mS | 18.3mS, 33.4mS | 12.89mS, 25.8mS |
| I_{D1}, I_{D5} | 2mA, 19.1mA | 1.43mA, 2.42mA | 1.44mA, 2.51mA | 0.872mA, 1.78mA |
| $g_m/I_{D1}, g_m/I_{D5}$ | 21.55 S/A, 3.93 S/A | 12.8 S/A, 13.4 S/A | 12.7 S/A, 13.3 S/A | 14.8 S/A, 13.5 S/A |
| f_c, PM | 66.6MHz | 66.6MHz, 75 $^\circ$ | 55.5MHz, 78.1 $^\circ$ | 50.09 MHz, 74.4$^\circ$ |
| Power | 165mW | 30.1mW (est) | 27.2mW | 18.67mW |
| DR | 91dB | 91 dB | 90.28 dB | 90.38 dB |
| t_s | 34.7nS | 32.4 nS | 33.3ns | 34.91 nS |
| $ \epsilon_s $ | 0.023% | 0.023% | 0.017% | 0.019% |

Table 2- MATLAB Calculated Values vs Simulation Values from the .op listing (*No HSPICE simulation)

The optimized c_1 and c_2 parameters greatly improved the parameters. The stage 1 load was lowered, as was C_c . This was achievable because the g_m 's were brought into more reasonable values, along with the decreased bias currents. While the first pass resulted in significant deviation from desired g_m/I_D values, the optimized version brought them back into line. To first order, the first pass simulation matches quite well to the MATLAB calculated values. As expected, the C_{stage} loads are 20% higher in HSPICE due to the additional parasitic junction capacitances at the drains, and thus f_c is lower. The g_m/I_D values match, as does the settling time. The lower ϵ_s indicates additional open-loop gain, which is an acceptable improvement. Additionally, the 30% current approximation for biasing was slightly conservative, as the first pass simulation shows a power draw of 27.2mW. The desired output common-mode was 1.5V, to allow for maximum swing between the rails. To ensure fast settling and stability of the common-mode output, the transconductance of the 'g' element was chosen to be comparable to the transconductance of M1, thus emulating the differential signal path. A transient analysis showed that the CM is stable, and an extended discussion of CMFB can be found later in this report.

To further optimize the circuit and to minimize power, I_{REF} and the m-factors for M3, M4, Mtail, and M6 were iterated to lower values. The motivation was to maintain similar I_{D1}/I_{D5} ratios as previously calculated, but use less current. Ultimately, g_m/I_{D1} was increased by 17% while g_m/I_{D5} stayed the same. This change lowered the V_{OV} of the input pair. As the current was lowered, the values of the nulling resistor and C_c were changed to fine tune to the step response. It was observed that a smaller C_c caused the transient to rise faster with a greater overshoot, but slightly increasing R_n allowed the waveform to still settle within the static error bounds. Great care was taken to ensure that $R_n < 1/g_{m5}$, thus avoiding LHP zeros. At the smaller C_c , the dynamic range decreased by ~ 0.5 dB due to greater noise power at the output. It can be argued that the design assumption to ignore the noise contribution from the cascode transistors and the nulling resistor was acceptable, seeing as the simulated $N_{tot, Vrms}$ varied between 1% and 3% of the calculated value. The output noise for the final optimized circuit was slightly elevated compared to the first pass same level as before despite a decrease in I_D and g_m due to the lower C_c and higher R_n , but still the dynamic range specification remained within bound.

Frequency Response: Bode Plot of $T(\omega)$

An AC analysis of the OTA was performed for the open-loop case, $T(\omega)$, and Figure 2 contains a Bode plot of the frequency response. The dominant pole created by the Miller compensation capacitor is clearly seen at approximately 10kHz, while the non-dominant pole can be more clearly seen in the phase plot, and occurs above 100 MHz. The Miller compensation capacitor achieved its purpose; the poles are split far enough to create the desired phase margin at the unity-gain frequency of the $T(\omega)$ (crossover frequency), which corresponds to the f_{-3dB} point of the closed-loop frequency response.

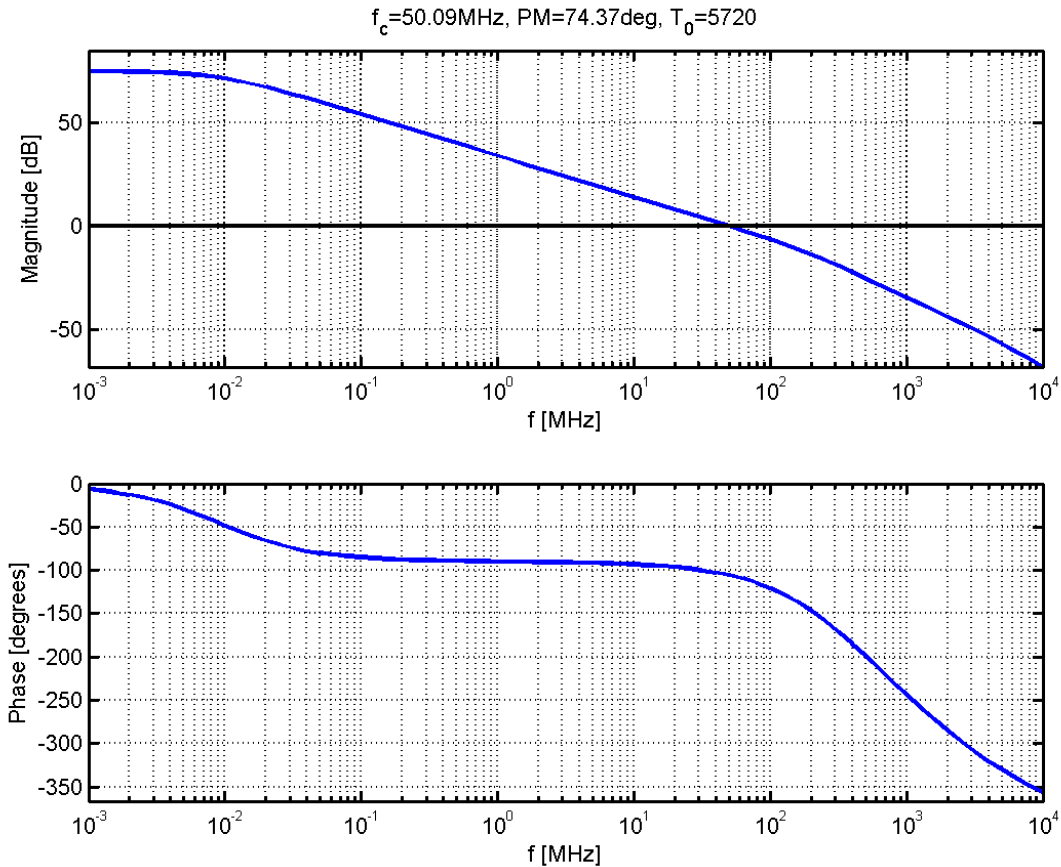


Figure 2 – Frequency response of the open-loop transfer function.

While additional poles exist due to the cascodes in the telescopic stage, these occur around f_t , well above the frequencies of interest for the operation of this OTA. It can be observed in this plot that the nulling resistor is working to mitigate the effects of the right-half-plane zero at g_{m5}/C_c caused by the output stage. If nothing were done to compensate for this zero, the gain would begin to noticeably flatten out between the dominant and non-dominant poles and the phase would drop by another 45° at that frequency.

Transient Analysis

Simulation of the transient response of the amplifier demonstrates the satisfied settling time and static error. Several observations can be made in Figure 3. First, a feed-forward effect is visible as downwards spike between 0 and 1 ns. Immediately following this region, the device enters slewing mode. Slewing accounts for most of the settling time of the amplifier. At around 27ns, the error between V_{od} and V_{id} decreases to within linear operating range, so the device follows a standard second-order settling response to a step impulse from that point forward. There is a brief overshoot, followed by a rapid damping of the oscillation. This optimal however, because the overshoot is the result a rapid rise time that decreases the overall settling time. The degree of damping and overshoot are controlled by the Miller compensation capacitor and the nulling resistor. C_c adjusts the degree to which the dominant and non-dominant poles are split, thus changing the second-order response

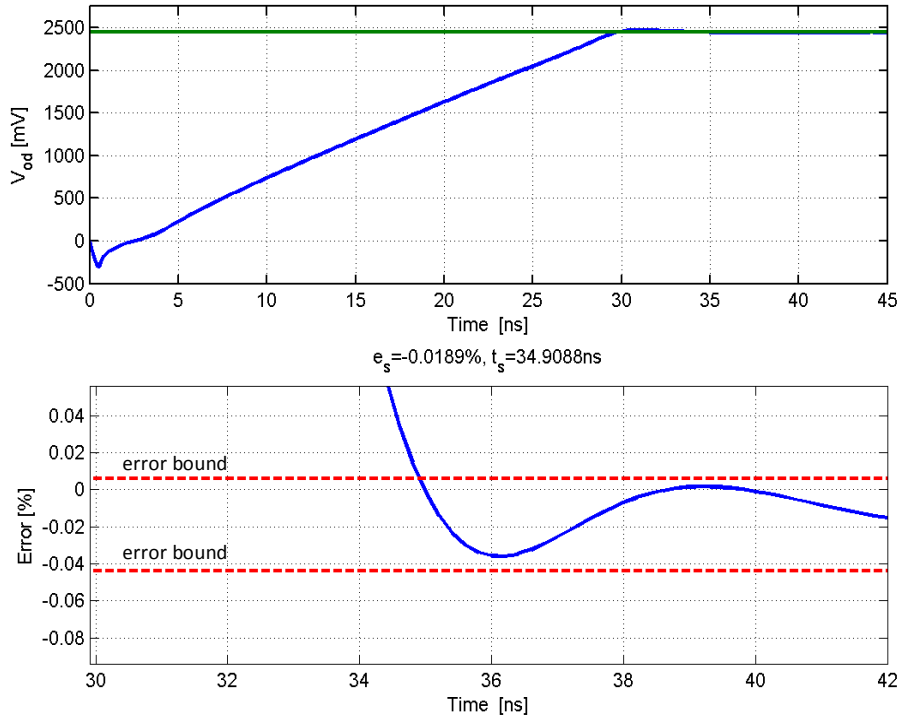


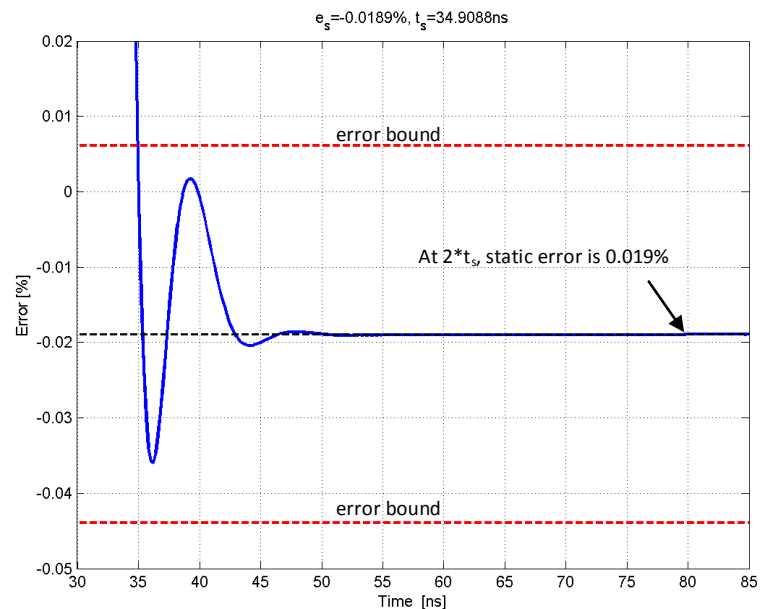
Figure 3 (left) – Top plot V_{od} transient response, with ideal value shown in green.

Bottom plot of Figure 3 shows percent static error versus time and is a zoomed-in view. This plot clearly shows how the transient settles within the specified error bounds in under the required settling time.

The settling time was significantly improved by ensuring the oscillations decay rapidly. This prevented the signal from crossing out of the desired static error specification after entering the appropriate range.

Decreasing C_c slowed the rise time, while increasing R_n improved the damping. Great care was made to ensure that the zero from the nulling resistor would stay in the right half plane. C_c and R_n were adjusted to provide the best settling time behavior and waveform for the chosen bias point.

Figure 4 (right) – Zoomed-out version of the static error plot, showing the settling at twice the specified settling time.



Common Mode Voltage Analysis

Fluctuations on the common mode can effect a change in the circuit's operating point, and through the feedback loop, output common mode voltages can even change the quiescent operating point of devices in the first stage. A CMFB loop is used to control and maintain it. For this purposes of this project, the V_{oc} sense circuit and common-mode feedback circuit are idealized. The $V_{DD}/2 = 1.5V$ common mode output voltage ensures maximum possible swing. A transient analysis of the common mode output voltage was performed, indicating a stable loop. The result is displayed in the t plot in Figure 8 below. The initial transient spike indicates the initial response to the step driving the amplifier. The circuit reacts through the common mode feedback loop, which injects or withdraws current from the tail node such that V_{oc} is driven back to the desired value, $V_{oc,des}$. The transconductance of the ideal 'g' element used to manage this tail current was chosen to ensure fast equalization while keeping the CMFB loop stable. Initially, the g_{cmfb} was chosen to match g_{m1} , to emulate the differential signal path loop. However, the second V_{oc} fluctuation recovery time was causing a higher settling time. The g_{cmfb} was thus increased, and the optimal value found was very similar to the tail transistor transconductance.

In the V_{oc} transient, another spike is visible at 30 ns. This spike represents the end of the slewing period. Note that the common mode settles back to its quiescent point at approximately the same time as the system settling time t_s .

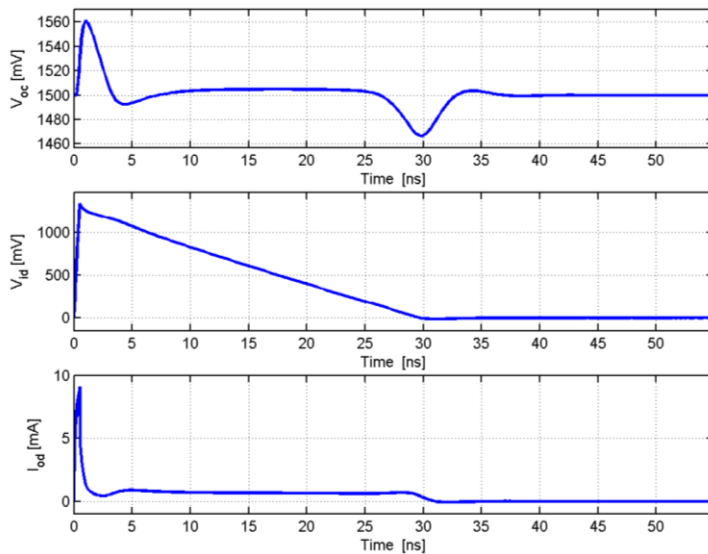


Figure 5 – Transient plot of V_{oc} , V_{id} , and I_{od} .

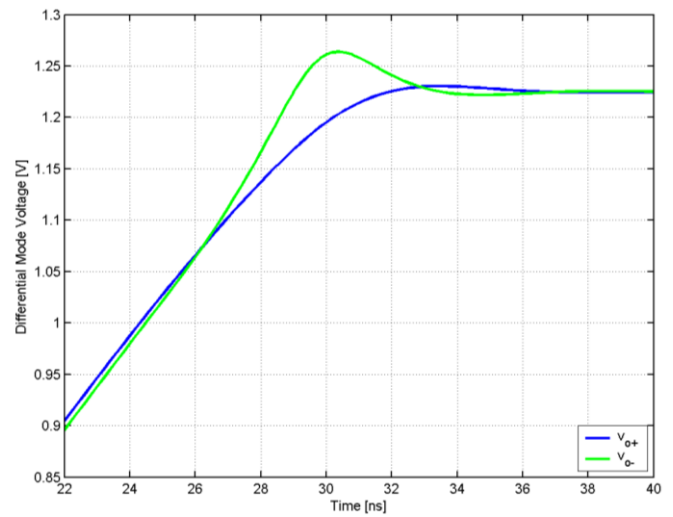


Figure 6 – V_{op} and V_{om} vs time

The V_{oc} plot in Figure 5 illustrates that the common mode output is stable and disturbances are quickly attenuated. The dip in the V_{oc} is explained by the deviation in the differential output voltages, shown in Figure 6. When V_{om} exceeds V_{op} starting at $t=27ns$, the $V_{oc} = (V_{op} - V_{om})/2$ decreases below the value it maintained in the region prior to $t=27ns$. As V_{om} returns to be almost equal to V_{op} , the V_{oc} increases back to the nominal value. This deviation is likely due to the different capacitive loads that the positive and negative signal branches see when at the full input step magnitude.

The second plot in Figure 5 shows the V_{id} transient. This voltage signal represents the input to our operational transconductance amplifier. It is derived from the driving step signal (sourced in our circuit simulations from V_{sd}), but also accounts for the feedback loop. Thus, the V_{id} can be thought of as the error between the desired level (V_{id}) and the actual output level (V_{od}). Note that it quickly rises, as the step input is applied; then, a linear fall-off region indicates the slewing. A significant portion of the settling time is spent slewing. This is contrary to what the hand calculations indicated. It was realized here that a significant conceptual error was made in the original formulation for the settling time calculation, account for both slewing and dynamic settling time. A simplified 'one stage' approach was taken. Though this gross oversimplification occurred during the design phase, the settling times did fall within specifications. Finally, the last plot on Figure 5 shows the current transient through the amplifier. Qualitatively, the current spikes when the input differential step is applied; current rapidly decreases, and drops to near zero when steady state is reached. Similar to the V_{id} plot, a small amount of I_{od} is present during slewing.

Noise Analysis

The dynamic range of our circuit is strongly affected by the noise power. The topology chosen provides acceptable noise performance for the given requirements, which demand a large open-loop gain for low settling error and high dynamic range. The total integrated noise power is approximated via an integral from 1 kHz to 100 GHz. This method focuses on our frequency range of interest, and provides a good quantitative approximation to the range (0 to ∞).

Flicker noise is the dominant effect until about 100 kHz. At this point, the noise plateaus before finally falling off around 100 MHz. Despite this, the total integrated noise does not accumulate in great quantity until approximately 10 MHz, because of the small absolute bandwidth over which flicker noise acts. The top chart in the figure below displays the noise power spectral density on a log-log scale; keeping in mind that the frequency axis is logarithmic, the integrated noise is not large in the flicker-noise regime.

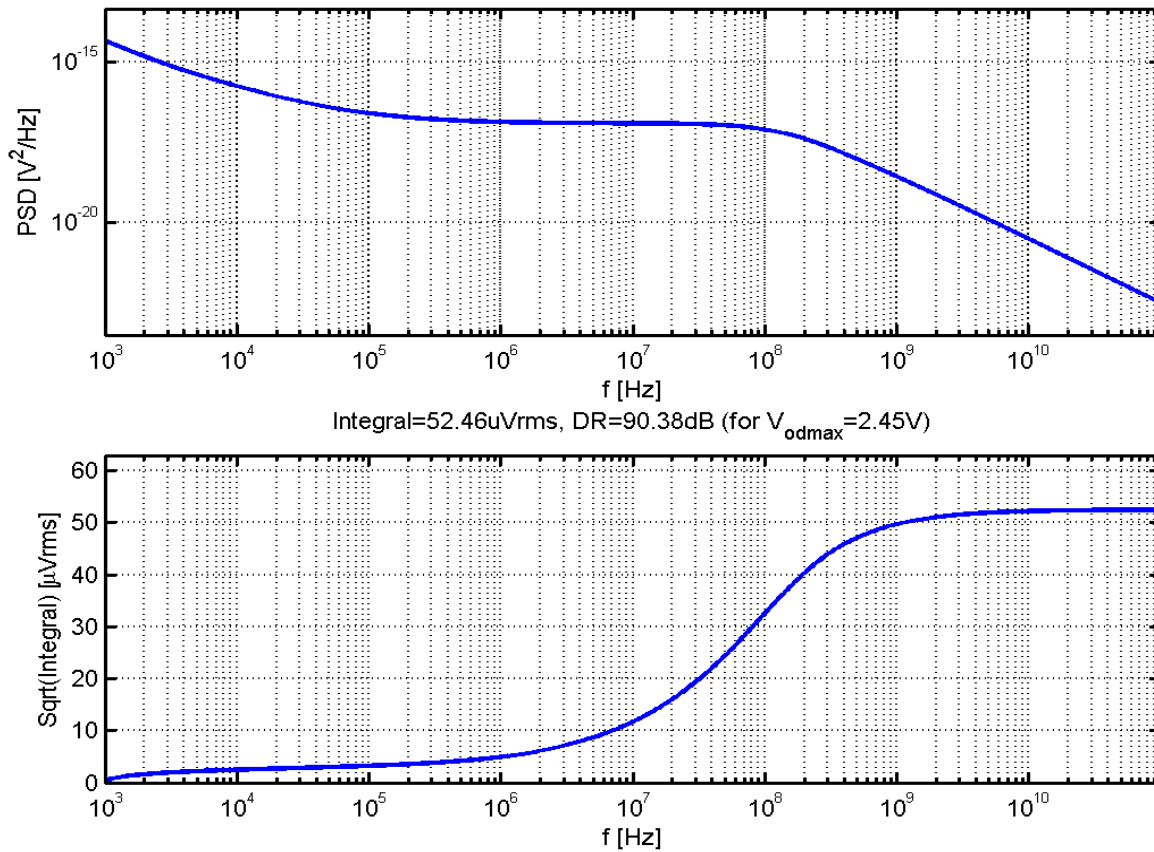


Figure 7 - Total integrated noise

Figure 7 displays the power spectral density and the total integrated noise, respectively, graphically illustrating the effect of the limited bandwidth with regards to the flicker noise. The noise that accumulates during the flicker noise dominated frequency range is insignificant compared to the noise after that range. Eventually the total integrated noise plateaus around 52 μV_{RMS} . The high frequency roll-off in the power spectral density and the corresponding plateau in the total integrated noise plot (bottom chart in the figure above), which starts between 100MHz and 200 MHz, correspond the region in which the closed-loop gain begins to approach unity. The roll-off is a reflection of the bandwidth of the entire amplifier.

Output Range

To operate linearly, the amplifier gain must remain fairly flat with respect to the output differential voltage. However, for the purposes of maximum dynamic range, it is desirable to have a high $V_{od,peak}$, thus boosting signal power with respect to noise power. For use in practical circuits, the maximum advisable input differential should result in no more than a 30% drop in gain, a drop that is caused by the output swing bringing the V_{DS} voltages in the output stage closer to or even into the triode region. The DC output range is shown below in Figure 8. The HSPICE simulator algorithm determines a DC operating point and assumes a linear model at that bias point. Therefore, additional caution is required to ensure that the chosen input step does not violate the advisable range of input differential step voltages. For the specified closed loop gain of 1, the maximum $V_{od,peak}$ is equivalent to the maximum advisable input differential step voltage.

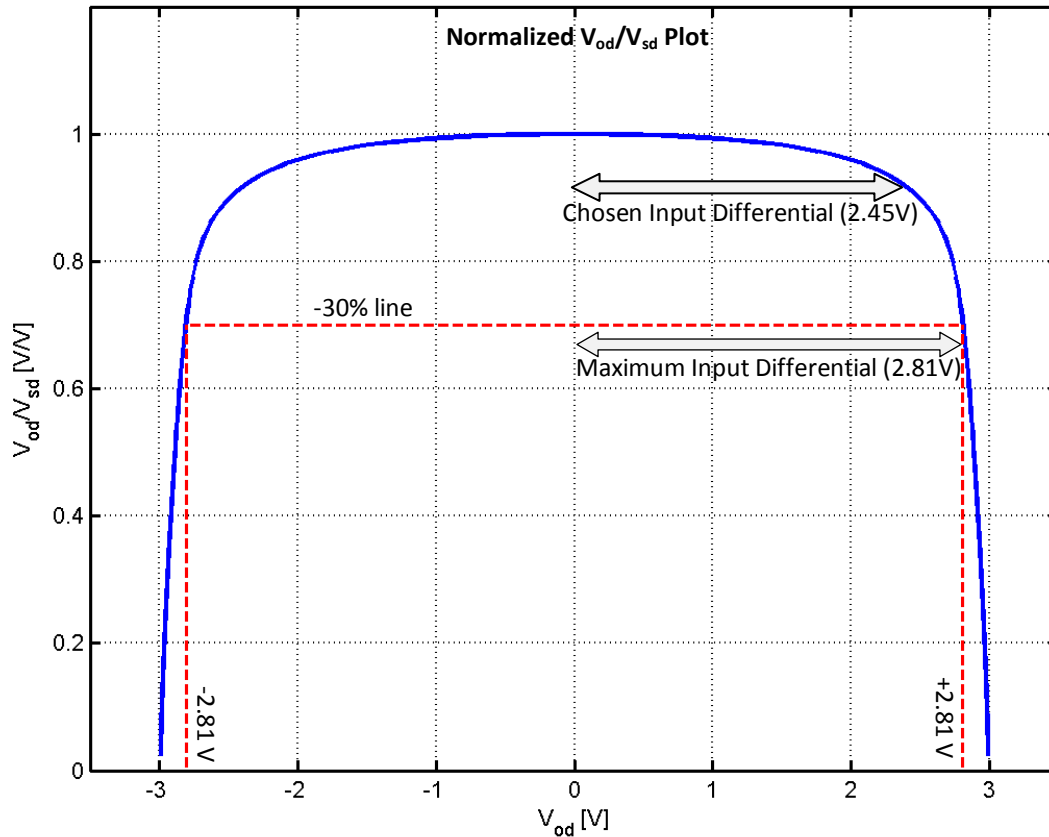


Figure 8 – Normalized plot of the output range, open loop DC gain V_{od}/V_{sd} of the amplifier vs V_{od} .

To determine this value, the DC operational range of the OTA was analyzed. A maximum $V_{od} = \pm 2.81$ V was attained. A value of 2.45V was chosen for simulation because it satisfied the dynamic range requirement while minimizing the settling time. As the OTA is subjected to a larger input step, the circuit must spend a longer time slewing.

Corner Simulations

Corner cases were simulated for the circuit using the process variation libraries for fast and slow transistors. To simulate worst-case corner phenomena, the slow corner had the OTA operating at high temperature (125°C) and the fast corner operated at 0°C. The nominal case, for comparison, was simulated at 25°C.

Though many device parameters change, the most significant differences between the fast and slow models are the gate oxidizer parameters. Thinning the gate oxide and boosting its dielectric constant slows the device by increasing effective C_{gg} - an aggregate effect primarily due to the higher C_{gd} and C_{gs} resulting from close spacing of the conductors. Conversely, for the fast process corner, the gate capacitance decreases, primarily due to thick oxide. These variations in C_{gg} , with range of $\pm 10\%$ seen in the operating point analyses, dramatically affects the frequency response of the total amplifier. Time constants along the entire signal path are significantly altered. Due to the design's healthy phase margin, stability was not a major issue as the signal-path poles varied. Furthermore, with a reasonable tolerance on the settling time for nominal case, the fast and slow corners obtained a t_s which was close to the desired value.

A notable feature is the decrease in intrinsic gain along the entire signal path, specifically in the devices M_1 and M_5 (the primary drivers for signal gain). Intrinsic gain $g_m r_o$ in these devices fluctuates; this is a combined result of the varying device parameters as well as the overdrive voltage. In the long-channel model, r_o is inversely proportional to drain current, and the decrease in drain current observed in the slow corner works to increase r_o , thus keeping the open-loop gain high. In the fast case, the elevated drain currents reduce r_o , and the open-loop gain drops below the 4000V/V needed to achieve a 0.025% static error. Overdrive voltage variations are largely due to the bias network. Notably, the trim resistors in the bias voltage generator circuitry do not track with process, and thus the overdrive voltage for the NMOS cascode is changed. This effect can be minimized by implementing all bias resistors as triode-mode transistors; for the purposes of this project, ideal resistors were chosen for simplicity. Comparative analysis of the cumulative intrinsic gain along the signal path (telescopic stage input M_1 , and second stage common source M_5) accounts for variations on the amplifier open loop gain of $\pm 25\%$.

Table 3 shows selected circuit parameters for nominal, slow, and fast corner cases, with percent deviation from nominal. Significant percent deviations, greater than $|20\%|$, are bolded for emphasis.

| Parameter | Nominal | Slow | Fast |
|-----------------------------|---------|----------------------|----------------------|
| Dynamic Range (dB) | 90.38 | 89.15 (-1.4%) | 90.75 (+0.4%) |
| Settling Time (ns) | 34.91 | 40.08 (+15%) | 38.46 (+10%) |
| Static Error (%) | -0.019 | -0.020 (+5.3%) | -0.030 (+58%) |
| Power (mW) | 18.67 | 17.21 (-7.8%) | 20.89 (+11.9%) |
| Closed Loop f_{3dB} (MHz) | 50.09 | 37.37 (-25%) | 60.63 (+21%) |
| Phase Margin | 74.37 | 73.99 (-0.5%) | 75.21 (+1%) |
| T_0 (Open Loop) | 5719.5 | 5874.5 (+2.7%) | 3628.9 (-37%) |
| Intrinsic Gain M_1 | 45.76 | 47.15 (+3%) | 42.68 (-7%) |
| Intrinsic Gain M_5 | 16.98 | 20.50 (+21%) | 13.54 (-20%) |
| Drain Current I_{D1} | 0.872mA | 0.785mA (-10%) | 1.01mA (+15%) |
| Drain Current I_{D5} | 1.78mA | 1.67mA (-6%) | 1.96mA (+10%) |

Table 3 – Selected parameters for nominal, slow, fast corner simulations.

The open loop gain is inversely proportional to the settling time error. Note that in the fast case, since T_0 falls below 4000, the OTA fails to meet the static settling error requirement, as determined through transient simulation. Figure 9 shows the frequency response of the open-loop gain of the fast and slow corners and displays the nominal case for comparison. In this form, it is evident that the fast corner has pushed the open-loop unity gain crossover frequency outward, at a slight cost to the dc open loop gain A_{v0} . The fact that the fast corner has a slightly wider bandwidth is understood because the gain has been reduced. Following the gain-bandwidth product, as gain decreases the bandwidth increases.

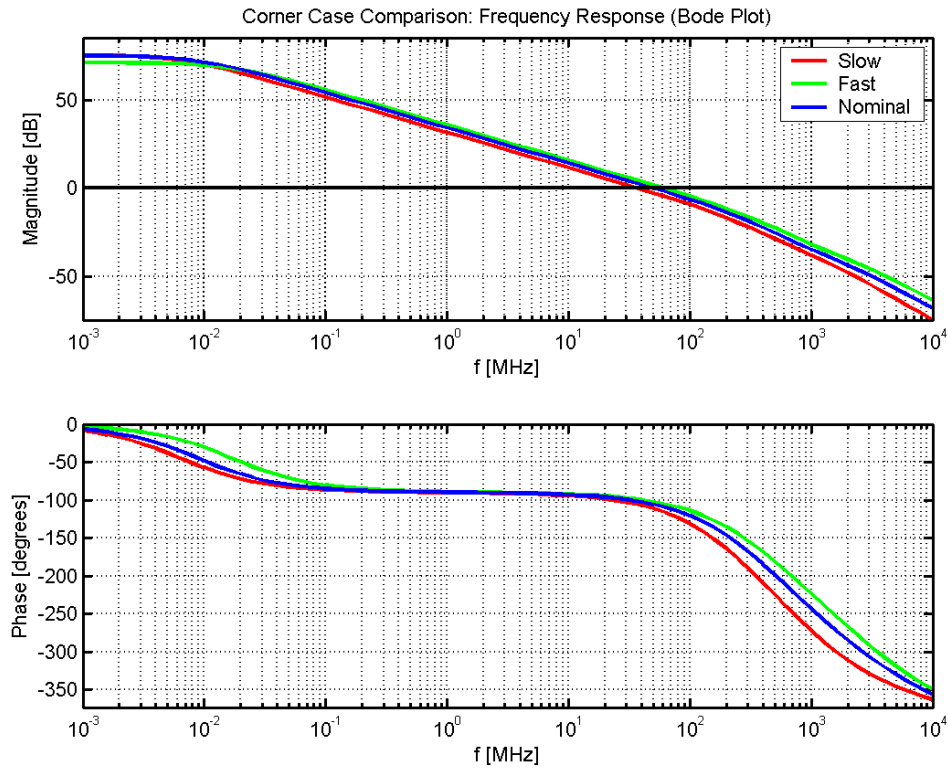


Figure 9 –Frequency response for nominal/fast/slow

Figure 10 shows the transient comparisons. A very important issue is the non-intuitive “slower” t_s obtained for our fast case. The fast corner’s more rapid rise time yields a stronger overshoot and thus takes slightly longer to enter the error bounds. A triode transistor for a nulling resistor would likely mitigate this effect.

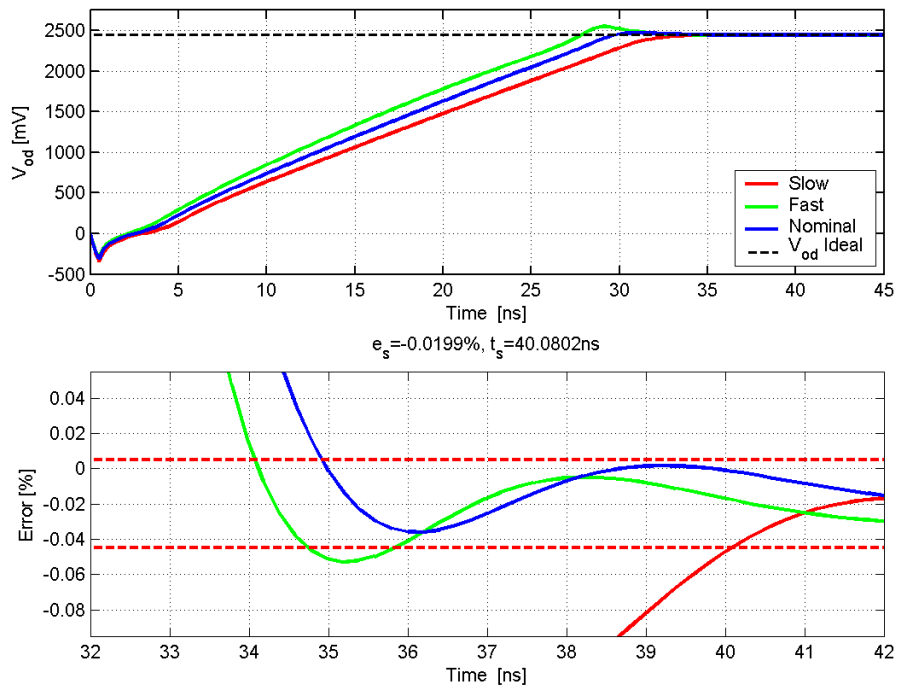


Figure 10 – Transient corner simulation comparison for V_{od} and percent error.

The slow corner does not overshoot and instead smoothly enters the error bound region. A lack of overshoot in this case corresponds to a slower rise time, and so the settling time increases.

Conclusion

This project served as an excellent opportunity to utilize the g_m/I_D design methodology in designing a practical circuit. Having never used this design paradigm before, it was a challenge that ultimately proved satisfying and productive. It allowed for rapid iteration and an intuitive understanding of the amplifier that we have not had before in earlier courses and projects. An initial literature review proved very useful in understanding the scope of this project, especially to gain insight into creating more complex topologies with the g_m/I_D approach. A list of sources we consulted are included in the References section below.

To streamline our design approach, we chose to base our design approach on circuits that have been shown for class examples, adding complexity and additional steps where we believed would increase accuracy for our specific topology. Certain parasitic capacitances and second-order effects were ignored, but later we analyzed the HSPICE simulations to confirm our assumptions.

As introduced in a previous section, late in the development of the amplifier, after we had already iterated several circuits that met the specifications, it was discovered that our initial formulation for the settling time calculation did not appropriately address the two-stage topology and the effective stage loading that is factored into the slew rate equation. The slewing time appeared to dominate the settling of our amplifier. We did an extensive study of the settling time issue, using [5] as a reference and using the values from our final operating point analysis, but we still found significant differences between first-order hand calculations and the simulated result. However, these differences were not great enough to move us “out of the ballpark”, and so settling time was met. Increasing the bias currents would have improved the slew rate, but this comes at the expense of additional power. Our design(s) were ultimately able to meet the specified settling time and static error requirements at lower power.

The bias network evolved over the course of our design, going from simple idealized sources to basic current mirrors to finally a wide swing cascode current mirror. A misunderstanding regarding the maximum allowable m-factors from a single diode-connected load forced a late-stage revision of the bias currents, increasing our power consumption. Fortunately, our extensive iterative design scripts allowed quick adjustment and optimization following this change. We chose to deviate from the usual biasing approach for the NMOS cascode transistors in the telescopic stage, because we noticed that additional devices to certain nodes were causing the settling time to increase. Thus, a bias voltage was generated using a V_t reference circuit that could stand apart from the other structures. While this is not an optimal approach (the large resistors used, while within bounds for our technology, take up a large amount of area), it proved satisfactory for the final performance of the circuit.

The last significant design challenge faced was the possibility of a left-half plane zero caused by the nulling resistor. Earlier design iterations had increasing the value of the nulling resistor to beyond $1/g_{m5}$, and improved the settling response by allowing for more rapid damping. We extensively studied this issue, running pole-zero analysis in HSPICE. We ultimately adjusted the value of the nulling resistor to ensure its placement near infinity in the right-half plane. Fortunately, our design was robust enough not to degrade significantly from this change.

This project allowed us to become more proficient in design tools, which we both felt excited about. We greatly appreciated the provided MATLAB analysis files and SPICE simulation files by the course instructor and teaching assistants. These scripts were expanded upon as we consolidated our entire design flow into MATLAB. By compartmentalizing the various analyses (AC, DC, transient, noise) into different SPICE decks, we were able to both simulate and analyze our circuit entirely with a single MATLAB command. Integrating our entire tool-chain, including an algorithmic generation of plots, greatly enhanced our productive and allowed us to focus on *analog design* aspect of this project.

In conclusion, this was a rewarding project and we learned a great deal about analog IC design. We were pleased that we met the specifications early, which gave us time to conduct further analysis and refinement to our design, primarily decreasing the power consumption of our circuit. This experience has given us the confidence to continue our studies into future analog IC courses.

References & Appendices

- [1] Libin Yao; Steyaert, M.; Sansen, W.; "Fast-Settling CMOS Two Stage Operational Transconductance Amplifiers and Their Systematic Design." IEEE Int'l Symposium on Circuits and Systems, 2002: ISCAS 2002. Volume 2, 26-29 May 2002. Pages(s) II-839-II-842.
- [2] Kashmiri, S.M.; Hedayati, H.; Shoaie, O.; "Systematic steps in design of a CMOS two-stage cascode-compensated OTA." Proceedings of the 15th Int'l Conference on Microelectronics. ICM 2003. 9-11 Dec. 2003. Page(s) 409-412.
- [3] Murmann, Boris. "EE 214 Course Reader: Analog Integrated Circuit Design." Fall 2007. Page(s) 246-257.
- [4] Cortes, Fernando Paixão and Sergio Bampi. "Miller OTA Design using a Design Methodology Based on the gm/Id and Early-Voltage Characteristics: Design Considerations and Experimental Results." Federal University of Rio Grande do Sul (UFRGS). Informatics Institute.
- [5] Lotfi, R.; Taherzadeh-Sani, M.; Yaser Azizi, M.; Shoaie, Omid; "A Low-Power Design Methodology for High Resolution Pipelined Analog-to-Digital Converters". Low Power Electronics and Design, 2003. Proceedings, ISLPED '03. 25-27 Aug. 2003. Pages:334-339

Final .OP Listing

```
**** voltage sources
subckt
element 0:vdd
volts 3.0000
current -6.2230m
power 18.6690m

***** current sources
subckt x1 xt
element 1:iref 4:it
volts 2.3094 0.
current 210.0000u 0.
power -484.9754u 0.

**** voltage-controlled current sources
subckt x1
element 1:g1
v drop 422.2367m
current 1.9317u

**** mosfets

subckt x1 x1 x1 x1 x1 x1
element 1:mnref1 1:mnref2 1:mnref3 1:mbp2a 1:mbp2b 1:mbp3a
model 0:nch214 0:nch214 0:nch214 0:pch214 0:pch214 0:pch214
region Saturati Saturati Saturati Linear Saturati Saturati
id 210.0000u 274.9635u 291.4043u -274.9635u -274.9635u -291.4043u
ibs 0. 0. 0. 0. 0. 0.
ibd 0. 0. 0. 0. 0. 0.
vgs 690.5935m 690.5935m 690.5935m -1.1511 -902.2405m -874.1833m
vds 690.5935m 1.8489 2.1258 -248.8532m -902.2405m -239.6195m
vbs 0. 0. 0. 0. 248.8532m 0.
vth 586.0863m 566.8042m 562.1945m -727.9861m -775.3977m -728.3213m
vdsat 105.2078m 115.6099m 118.1319m -390.8808m -165.6929m -177.7988m
vod 104.5071m 123.7893m 128.3989m -423.1076m -126.8428m -145.8620m
```

| | | | | | | |
|---------|-----------|-----------|-----------|-----------|-----------|-----------|
| beta | 33.1912m | 33.1623m | 33.1553m | 4.2257m | 21.2772m | 21.3075m |
| gam eff | 894.1238m | 894.1238m | 894.1238m | 472.5709m | 468.1963m | 472.5709m |
| gm | 3.0138m | 3.6117m | 3.7456m | 826.0401u | 2.9663m | 2.8168m |
| gds | 56.9354u | 58.3951u | 60.5129u | 680.2731u | 57.3010u | 216.0906u |
| gmb | 687.8085u | 801.0536u | 825.1254u | 186.2786u | 613.2275u | 636.4444u |
| cdtot | 75.6351f | 60.9812f | 58.9180f | 81.4456f | 284.8254f | 352.6616f |
| cgtot | 82.8862f | 83.7000f | 83.8458f | 76.9351f | 367.4147f | 370.7921f |
| cstot | 159.7540f | 160.7364f | 160.8946f | 125.7226f | 576.4101f | 617.5406f |
| cbtot | 179.9211f | 165.3387f | 163.2899f | 133.3895f | 550.5024f | 660.7609f |
| cgs | 56.4323f | 57.1409f | 57.2484f | 53.9167f | 272.7646f | 272.0965f |
| cgd | 10.9247f | 10.9125f | 10.9103f | 18.5568f | 71.3731f | 71.3338f |

| | | | | | | |
|---------|------------|-----------|-----------|-----------|------------|------------|
| subckt | x1 | x1 | x1 | x1 | x1 | x1 |
| element | 1:m3p3b | 1:m3n1 | 1:m3n2 | 1:m3tail | 1:m3a | 1:m3b |
| model | 0:pch214 | 0:nch214 | 0:nch214 | 0:nch214 | 0:nch214 | 0:nch214 |
| region | Saturati | Saturati | Saturati | Saturati | Saturati | Saturati |
| id | -291.4043u | 104.8957u | 28.0643u | 1.7426m | 872.2699u | 872.2699u |
| ibs | 0. | 0. | 0. | 0. | 0. | 0. |
| ibd | 0. | 0. | 0. | 0. | 0. | 0. |
| vgs | -911.4742m | 1.4032 | 1.0199 | 690.5935m | 777.7633m | 777.7633m |
| vds | -634.5638m | 2.4231 | 1.5968 | 422.2367m | 201.4214m | 201.4214m |
| vbs | 239.6195m | 0. | -1.4032 | 0. | -422.2367m | -422.2367m |
| vth | -776.5715m | 522.8249m | 928.7678m | 590.5536m | 688.8621m | 688.8621m |
| vdsat | -171.6602m | 558.0239m | 113.8126m | 102.8411m | 103.7070m | 103.7070m |
| vod | -134.9027m | 880.3920m | 91.0886m | 100.0398m | 88.9012m | 88.9012m |
| beta | 21.2805m | 387.6061u | 4.5143m | 298.7801m | 168.0687m | 168.0687m |
| gam eff | 468.3489m | 894.1238m | 962.7276m | 894.1238m | 918.4534m | 918.4534m |
| gm | 3.0422m | 215.0706u | 419.9277u | 25.4484m | 12.8899m | 12.8899m |
| gds | 72.4680u | 281.0547n | 2.4883u | 614.8566u | 758.9696u | 758.9696u |
| gmb | 630.6990u | 64.0332u | 73.1483u | 5.8478m | 2.3662m | 2.3662m |
| cdtot | 299.9187f | 2.8075f | 11.5651f | 739.6672f | 382.2358f | 382.2358f |
| cgtot | 368.6202f | 8.3709f | 22.6191f | 743.7565f | 409.3704f | 409.3704f |
| cstot | 579.2100f | 13.4212f | 31.2697f | 1.4349p | 687.3236f | 687.3236f |
| cbtot | 566.9255f | 10.0172f | 26.0686f | 1.6781p | 785.3280f | 785.3280f |
| cgs | 274.1155f | 7.1347f | 17.5189f | 505.7459f | 285.5363f | 285.5363f |
| cgd | 71.3591f | 450.9153a | 2.3308f | 98.3563f | 54.2839f | 54.2839f |

| | | | | | | |
|---------|------------|------------|------------|------------|------------|------------|
| subckt | x1 | x1 | x1 | x1 | x1 | x1 |
| element | 1:m2a | 1:m2b | 1:m3a | 1:m3b | 1:m4a | 1:m4b |
| model | 0:nch214 | 0:nch214 | 0:pch214 | 0:pch214 | 0:pch214 | 0:pch214 |
| region | Saturati | Saturati | Saturati | Saturati | Saturati | Saturati |
| id | 872.2699u | 872.2699u | -872.2699u | -872.2699u | -872.2699u | -872.2699u |
| ibs | 0. | 0. | 0. | 0. | 0. | 0. |
| ibd | 0. | 0. | 0. | 0. | 0. | 0. |
| vgs | 779.5589m | 779.5589m | -914.4353m | -914.4353m | -874.1833m | -874.1833m |
| vds | 1.6500 | 1.6500 | -489.7059m | -489.7059m | -236.6584m | -236.6584m |
| vbs | -623.6581m | -623.6581m | 236.6584m | 236.6584m | 0. | 0. |
| vth | 697.8622m | 697.8622m | -777.6338m | -777.6338m | -728.3558m | -728.3558m |
| vdsat | 100.9668m | 100.9668m | -173.0693m | -173.0693m | -177.7728m | -177.7728m |
| vod | 81.6966m | 81.6966m | -136.8015m | -136.8015m | -145.8275m | -145.8275m |
| beta | 168.4393m | 168.4393m | 63.8447m | 63.8447m | 63.9226m | 63.9226m |
| gam eff | 928.6412m | 928.6412m | 468.3980m | 468.3980m | 472.5709m | 472.5709m |
| gm | 13.7102m | 13.7102m | 9.0115m | 9.0115m | 8.4215m | 8.4215m |
| gds | 263.0542u | 263.0542u | 262.3231u | 262.3231u | 664.3034u | 664.3034u |
| gmb | 2.2012m | 2.2012m | 1.8702m | 1.8702m | 1.9029m | 1.9029m |
| cdtot | 287.5529f | 287.5529f | 928.3977f | 928.3977f | 1.0590p | 1.0590p |
| cgtot | 404.5162f | 404.5162f | 1.1066p | 1.1066p | 1.1124p | 1.1124p |
| cstot | 651.4332f | 651.4332f | 1.7398p | 1.7398p | 1.8526p | 1.8526p |
| cbtot | 658.2595f | 658.2595f | 1.7307p | 1.7307p | 1.9833p | 1.9833p |

| | | | | | | |
|-----|-----------|-----------|-----------|-----------|-----------|-----------|
| cgs | 281.2156f | 281.2156f | 823.1573f | 823.1573f | 816.2764f | 816.2764f |
| cgd | 54.0785f | 54.0785f | 214.0684f | 214.0684f | 214.0016f | 214.0016f |

| subckt | x1 | x1 | x1 | x1 |
|---------|------------|------------|-----------|-----------|
| element | 1:m5a | 1:m5b | 1:m6a | 1:m6b |
| model | 0:pch214 | 0:pch214 | 0:nch214 | 0:nch214 |
| region | Saturati | Saturati | Saturati | Saturati |
| id | -1.7846m | -1.7846m | 1.7846m | 1.7846m |
| ibs | 0. | 0. | 0. | 0. |
| ibd | 0. | 0. | 0. | 0. |
| vgs | -726.3643m | -726.3643m | 690.5935m | 690.5935m |
| vds | -1.5001 | -1.5001 | 1.4999 | 1.4999 |
| vbs | 0. | 0. | 0. | 0. |
| vth | -684.3145m | -684.3145m | 572.6136m | 572.6136m |
| vdsat | -107.3158m | -107.3158m | 112.4484m | 112.4484m |
| vod | -42.0498m | -42.0498m | 117.9798m | 117.9798m |
| beta | 378.3730m | 378.3730m | 232.1977m | 232.1977m |
| gam eff | 472.5709m | 472.5709m | 894.1238m | 894.1238m |
| gm | 25.8140m | 25.8140m | 24.0861m | 24.0861m |
| gds | 564.0958u | 564.0958u | 395.0879u | 395.0879u |
| gmb | 5.7268m | 5.7268m | 5.3881m | 5.3881m |
| cdtot | 4.0451p | 4.0451p | 448.8228f | 448.8228f |
| cgtot | 4.5949p | 4.5949p | 584.4451f | 584.4451f |
| cstot | 8.0321p | 8.0321p | 1.1235p | 1.1235p |
| cbtot | 8.4864p | 8.4864p | 1.1792p | 1.1792p |
| cgs | 3.0420p | 3.0420p | 398.8248f | 398.8248f |
| cgd | 1.0742p | 1.0742p | 76.4091f | 76.4091f |